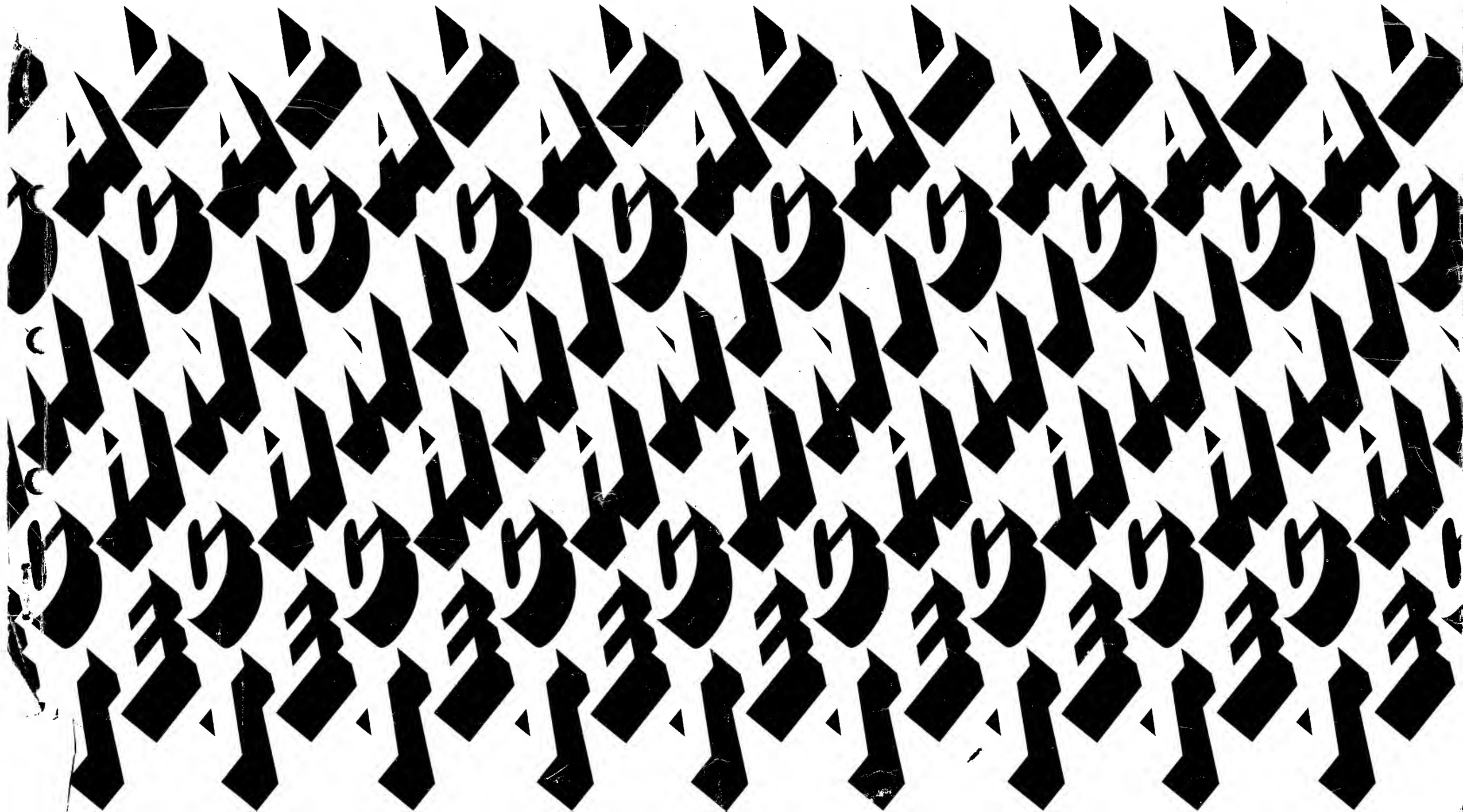
Computervision

CGP-100 Graphics Processor

Logic Diagrams



Document Control Number: 23- 00838
Issue Date _____

CGP-100 Graphics Processor

Logic Diagrams

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Order No. 001-00523-004

REVISIONS

SYM	ECO NO.	CHK	APPR'D		SYM	ECO NO.	CHK	APPR'D	
A	REL#2601			1/4/78					
B	#2887			10/78					
C	#3386			5/80					

COMPUTERVISION CORPORATION

L21X009 C REV.

NEXT ASSEMBLY	QTY
MODULE LIST	—

TITLE CGP-100 ELECTRONIC DOCUMENTATION PACKAGE

MODULE CGP

DRN D. DAVIDSON SHT 1 OF 1

ITEM	DRAWING OR PART NUMBER	STOCK NUMBER	QTY 01	QTY 02	DESCRIPTION (REF. DES.)	MANUFACTURER	NOTE/COMMENTS
1	L21X009		REF		DOCUMENTATION PACKAGE		NO DRAWING
2	DA21E120		1		CPU ASSY		
3	DS21E122		1		CPU SCHEMATIC		
4	DA21E130		1		CONTROL PANEL ASSY		
5	DS21E132		1		CONTROL PANEL SCHEMATIC		
6	ES21E050		1		BACKPLANE SCHEMATIC		
7	DA21E105		1		MUC ASSY		
8	DS21E107		1		MUC SCHEMATIC		
9	DA21E115		1		FPU ASSY		
10	DS21E117		1		FPU SCHEMATIC		
11	~~DA21E100~~		~~1~~		~~32K MEMORY ASSY~~		
12	~~DS21E102~~		~~1~~		~~32K MEMORY SCHEMATIC~~		
13	DS21E015		1		CPU FLOW CHART		
14	AH21H305		1		CPU MICROCODE LISTING		
15	AH21H315		1		FPU MICROCODE LISTING		
16	DA21E225		1		128K/32K MEMORY ASSY		
17	DS21C227		1		128K/32K MEMORY SCHEMATIC		
18							
19							
20							

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DS21E227 (9 Sheets) (OBSOLETE)

32K Memory Unit (Single Port) (Rev. D)
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Memory Management and Protection Unit (Rev. K)
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CGP Family Tree

CGP 100 COMPUTER A21C100

POWER MODULE AC14R422-01 50 Hz.

POWER MODULE AC14R422-02 60 Hz.

- BACK PLANE ASSY EA21E055
  - BACK PLANE DT21E056
- CARD FRAME ASSY A21E060
  - CARD GUIDE TOP EP21M152
  - CARD GUIDE BOTTOM EP21M153
  - END PLATE LEFT CP21M154-01
  - END PLATE RIGHT CP21M154-02
  - SPACER, BACKPLANE AP21M182
  - INTERFACE PANEL BRKT. CP21M174
  - TERMINAL INTERFACE PNL DP21M173
  - FRAME EP21E150
  - CARD GUIDE DP21E151
  - CARD SUPPORT DP21M158
  - POWER BOX ASSY A21M175
    - POWER BOX DP21M167
    - I/O S CABLE CA21E220
    - TTY CABLE CA21E215
    - POWER CABLE ASSY CA21E135
  - FACE PLATE ASSY A21M170
    - FACE PLATE DP21M165
    - WINDOW BP21M166
- CONTROL PANEL ASSY A21E130
  - CONTROL PNL ARTWORK DT21E131
- PWR SUPPLY AC21M020
- CGP 100 OPERATORS GUIDE 001-0203
- CABLE SET A21E111
  - CONTROL PNL CABLE (2) A21E090 — C-102
  - PWR SUPPLY CABLE CA21E070-01 — J-1CC
  - PWR SUPPLY CABLE CA21E070-02 — J-2CC
  - PWR SUPPLY CABLE CA21E070-03 — J-3CC
  - SIGNAL CABLE BA21E145 — C-103
  - GROUND CABLE CGP CA21E066-01
  - GROUND CABLE TELEFILE CA21E066-02
  - GROUND CABLE DISC CA21E066-03
  - GROUND CABLE TAPE DRIVE CA21E066-04
  - GROUND CABLE USERS CA21E066-05
  - © CC 150 INTERNAL BACKPLANE CABLE CA21E086
- ACCESSORIES LIST L21X008
  - EXTENDER BOARD DT21E057
  - EXTENDER CABLE CA21E065
- DOCUMENTATION PACKAGE L21X009 (REF)

MODULE LIST

- © CGP MEMORY(4) DA21E225
- CGP MUC DA21E105
- CPU CARD A21E120
- FLOATING POINT A21E115
  - EXTENDER BOARD - 15 IN. DA21E075
- MEMORY 128K/32K DA21E225

REF.

- IOS CONTROLLER EA14E1002

DX21Y007 D

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY

DRN T. Nilsen 8/12
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	CHK	APPD	DAT
D	ECO# 3195			
C	ECO #3126			
B	ECO #3004			
A	REL ECO #2594			

TITLE: FAMILY TREE CGP

SCALE —
DWG NO. DX21Y007
UNIT WT. —
SHEET 1 OF 1 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

REV A = REV 4

H+E 7851

Backplane

Connector List
Artwork Silkscreen

POWER SUPPLY CONNECTORS

TTY CONNECTOR

J1, J2, J4, J5, J6

PUNCH

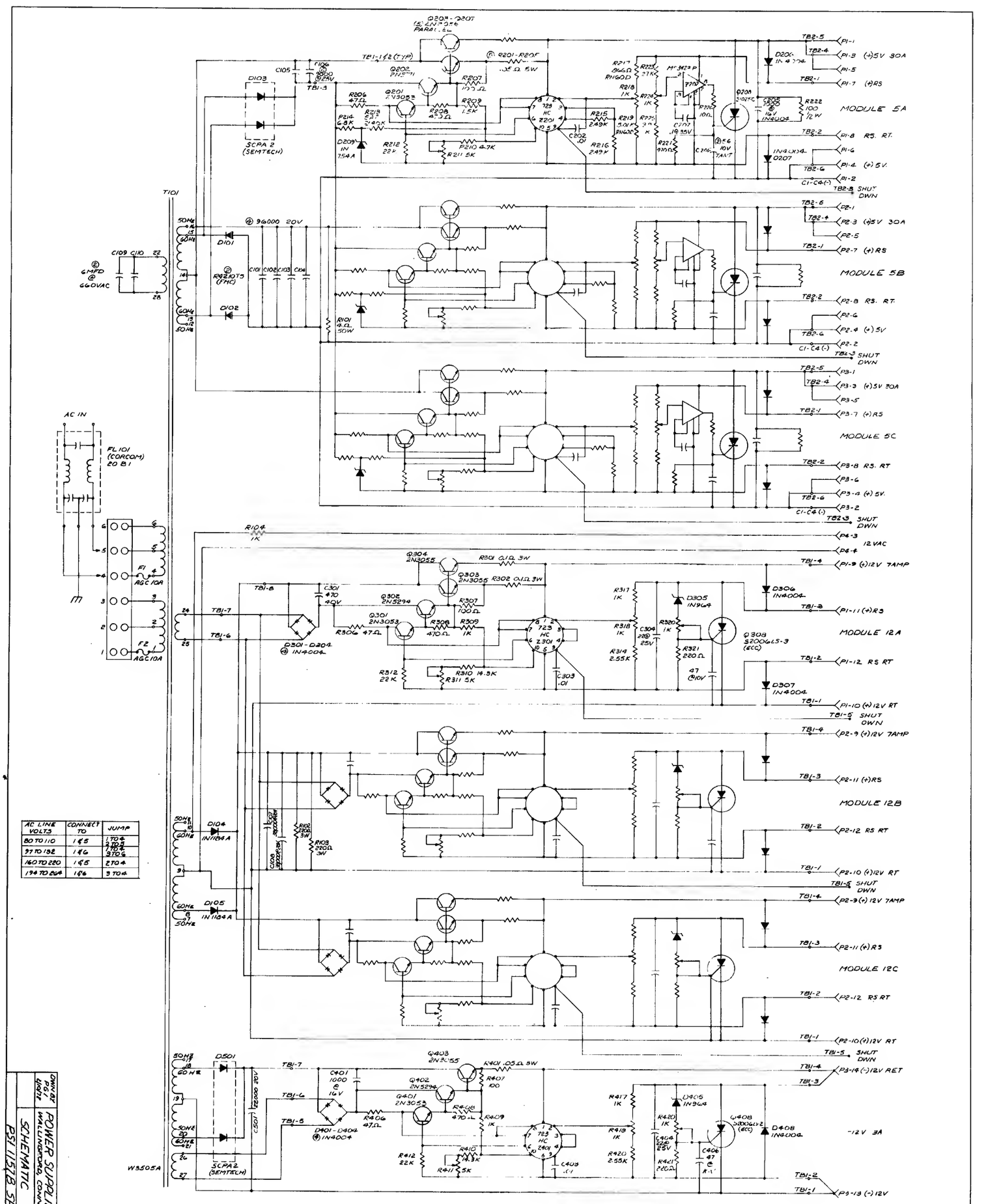
HI SPEED READER

TYPE	SLOT NO'S	CONN
TTY	1	J1
	5	J2
	13	J4
TTY	17	J5
	21	J6
10S	4	J9
	8	J10
	12	J11
	16	J12
	20	J13
10S	24	J14
PTP	5	J7
PTR	5	J8
MUC	2	
MUC	10	
MUC	18	
FPU	5	
FPU	11	
FPU	18	

10S J9-J14

Power Supply

	Sheet No.
Transformer	1
Regulator Modules	1
Logic Module	2
−5 Volt Regulator	2



AC LINE VOLTS	CONNECT TO	JUMP
80 TO 110	1 & 5	1 TO 4, 2 TO 5
97 TO 132	1 & 6	1 TO 4, 3 TO 6
160 TO 220	1 & 5	2 TO 4
194 TO 264	1 & 6	3 TO 4

DWN BY PG 1 1/1/78

POWER SUPPLIES
WALLINGFORD, CONN.

SCHEMATIC

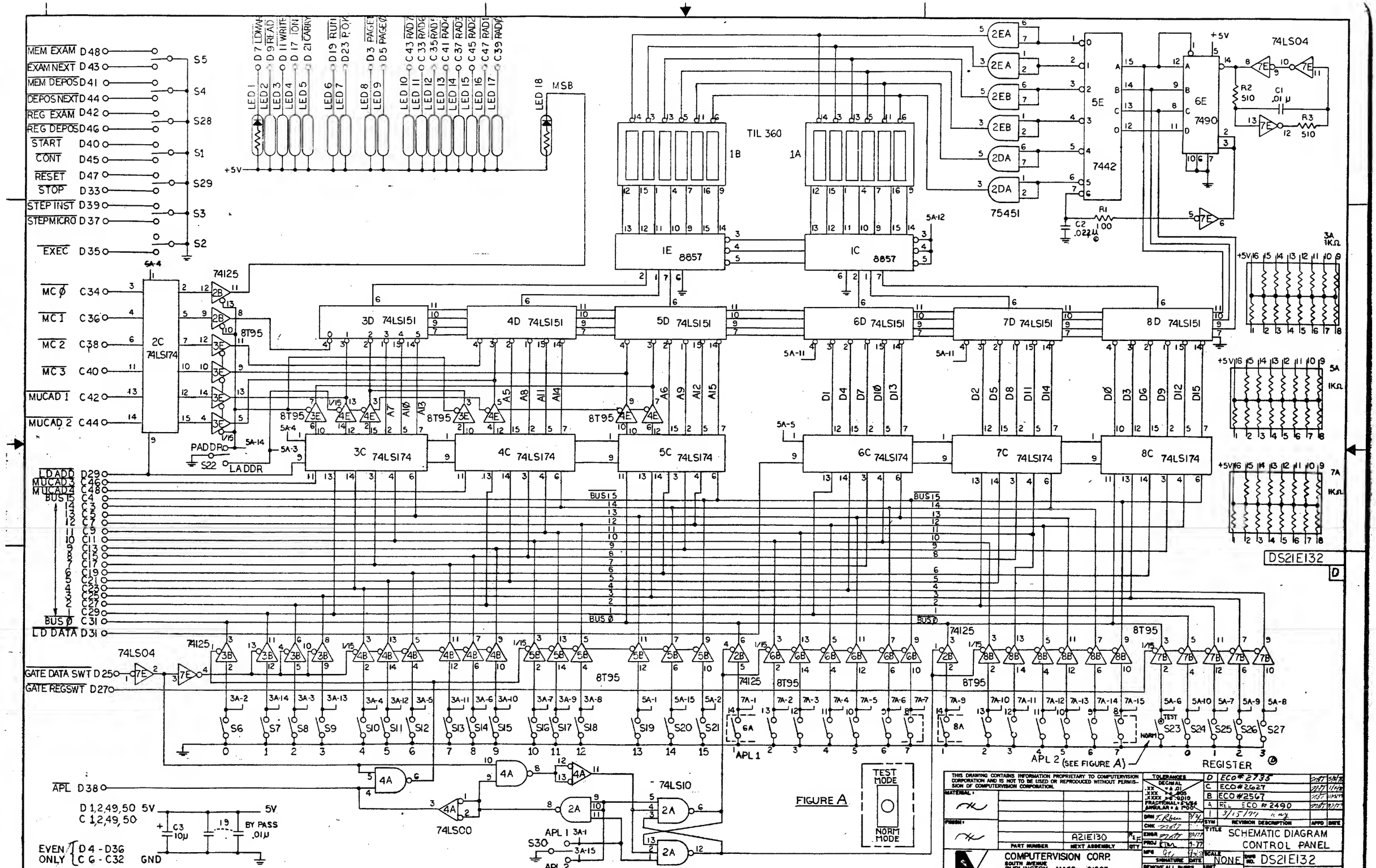
PSI 1157B SH1

+4.7V REF
A601 LM339
VCC +15V
+5V (A) 5 RG07 2.2K
RG08 150K
+5V(B) 6 RG09 2.2K
RG10 150K
+5V(C) 7 RG11 2.2K
RG12 150K
11 Y1
12 Y2
13 Y3
+11.3V REF
A602 LM339
VCC +15V
+12V(A) 8 RG13 2.2K
RG14 470K
+12V(B) 9 RG15 2.2K
RG16 470K
+12V (C) 10 RG17 2.2K
RG18 470K
D619 IN914
D620 IN914
D621 IN914
PCG01 TIL 112
RG29 470Ω
RG31 10K
RG22 1K
RG21 2.49K
A603 LM339
-12V
-5.5 V REF
RG19 3.24K
RG04 2.2K
RG20 470K
D610 IN914 B
RG32 1K
-12V
VCC +15V
RG30 680Ω
D609 IN4004 OR IN914
22Ω RG25
RG24 100K
DG11 IN914 B
PCG02 TIL 112
RG33 4.7K
-5V 21 RG23 22K
RG26 4.7K
RG28 470Ω
RG27 68K
RG34 1K
2N3053
DG12 IN914 B
-12V
N.C. THM. SW 100°C
20
N.C. REMOTE SHUT DWN
-12V
AC IN 2
FRM +12UPV 3
RAW +12 4
D601 - D606 @ IN4004
Z601 7815UC
C601 100 @ 16V
C602 22 @ 25V
C603 22@ 25V
RG42 3.01K RN60D
RG01 200Ω
RG43 1.4K RN60D
+4.7 REF
RG41 1.82K RN60D
RG02 1K
RG03 7.68K RN60D
VCC +15V
11.3V REF
1
R605 200Ω
C606 15 @ 20V TANT
R606 2K RN60D
C604 15 @ 20V TANT
C605 15 @ 20V TANT
-12V IN
GND IN OUT
79L05
(-)5.5V REF
LM320K -05
Z602
21 -5V OUT 1A
RG35 1K DG13 14 +5V (A)
RG36 1K DG14 15 +5V (B)
RG37 1K DG15 16 +5V (C)
RG38 2.2K DG16 17 +12V (A)
RG39 2.2K DG17 18 +12V (B)
RG40 2.2K DG18 19 +12V (C)
IN4004 OR IN914
SHUTDOWN OUTPUTS

DWN BY PGJ 2/10/78	POWER SUPPLIES WALLINGFORD, CONN.
	SCHEMATIC - LOGIC
	PSI 1157B SH2

Control Panel

Logic Diagram



MEM EXAM D48
EXAM NEXT D43
MEM DEPOS D41
DEPOS NEXT D44
REG EXAM D42
REG DEPOS D46
START D40
CONT D45
RESET D47
STOP D33
STEP INST D39
STEP MICRO D37
EXEC D35
MC Ø C34
MC 1 C36
MC 2 C38
MC 3 C40
MUCAD 1 C42
MUCAD 2 C44
LD ADD D29
MUCAD 3 C46
MUCAD 4 C48
BUS 15 C4
BUS Ø C31
LD DATA D31
GATE DATA SWT D25
GATE REGSWT D27
APL D38
D 1,2,49,50 5V
C 1,2,49,50
EVEN ONLY D4 - D36 C6 - C32
GND
5V
BY PASS .01μ
C3 10μ
MSB
TIL 360
1B
1A
1E 8857
1C 8857
2C 74LS174
3D 74LS151
4D 74LS151
5D 74LS151
6D 74LS151
7D 74LS151
8D 74LS151
3C 74LS174
4C 74LS174
5C 74LS174
6C 74LS174
7C 74LS174
8C 74LS174
74125
8T95
74LS04
74LS00
74LS10
75451
7442
5E
6E 7490
74LS04
R1 100
C2 .022μ
R2 510
C1 .01μ
R3 510
3A 1KΩ
5A 1KΩ
7A 1KΩ
DS21E132
APL 1
APL 2 (SEE FIGURE A)
REGISTER
TEST MODE
NORM MODE
FIGURE A
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
A21E130
PART NUMBER
NEXT ASSEMBLY
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
D ECO#2735
C ECO#2627
B ECO#2567
A REL ECO #2490
1 3/15/77
REVISION DESCRIPTION
TITLE SCHEMATIC DIAGRAM CONTROL PANEL
SCALE NONE
DWG NO. DS21E132
SHEET 1 OF 1 SHEETS

Central Processor Unit

	Sheet No.
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CPU Clock	5
FPLAs	6
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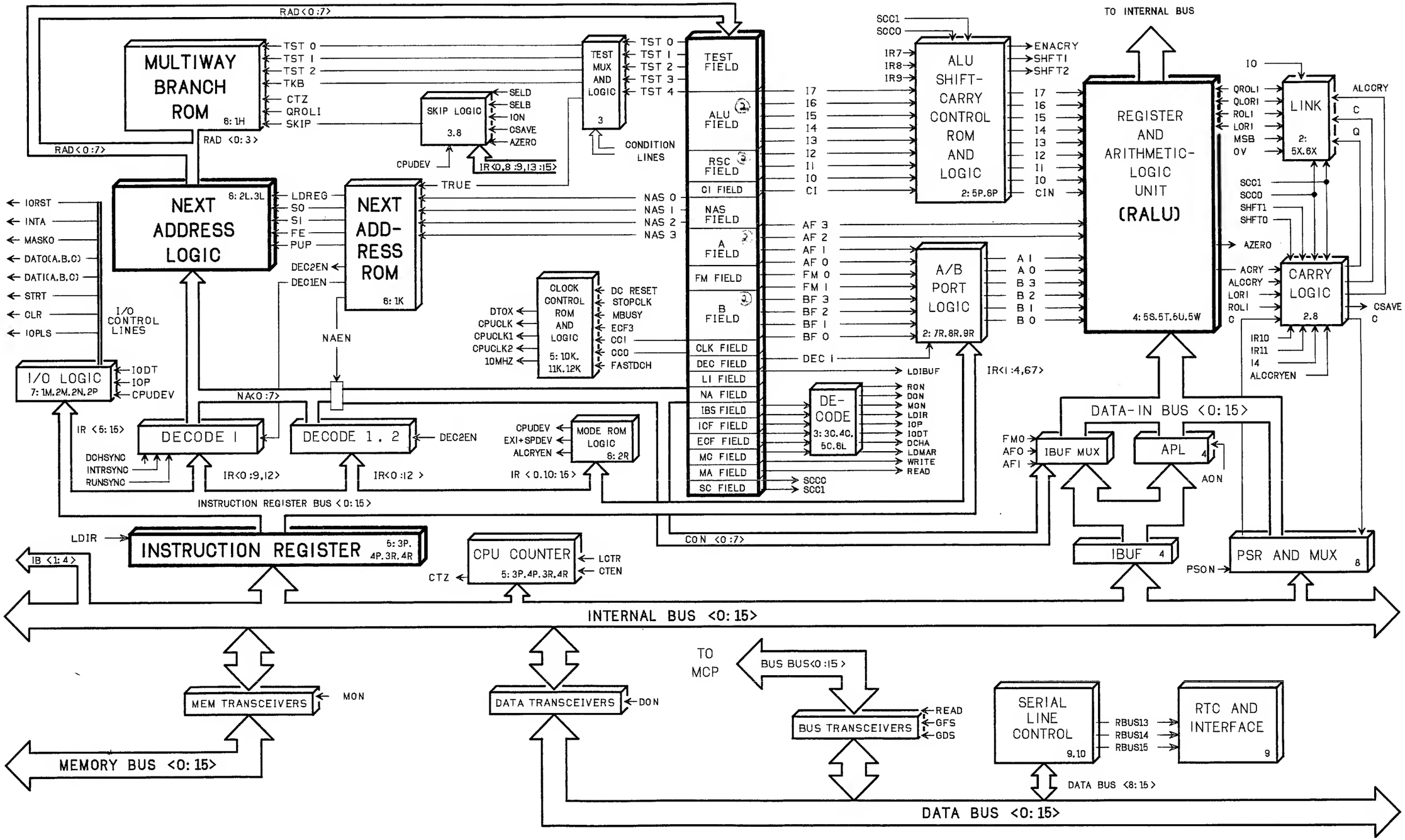
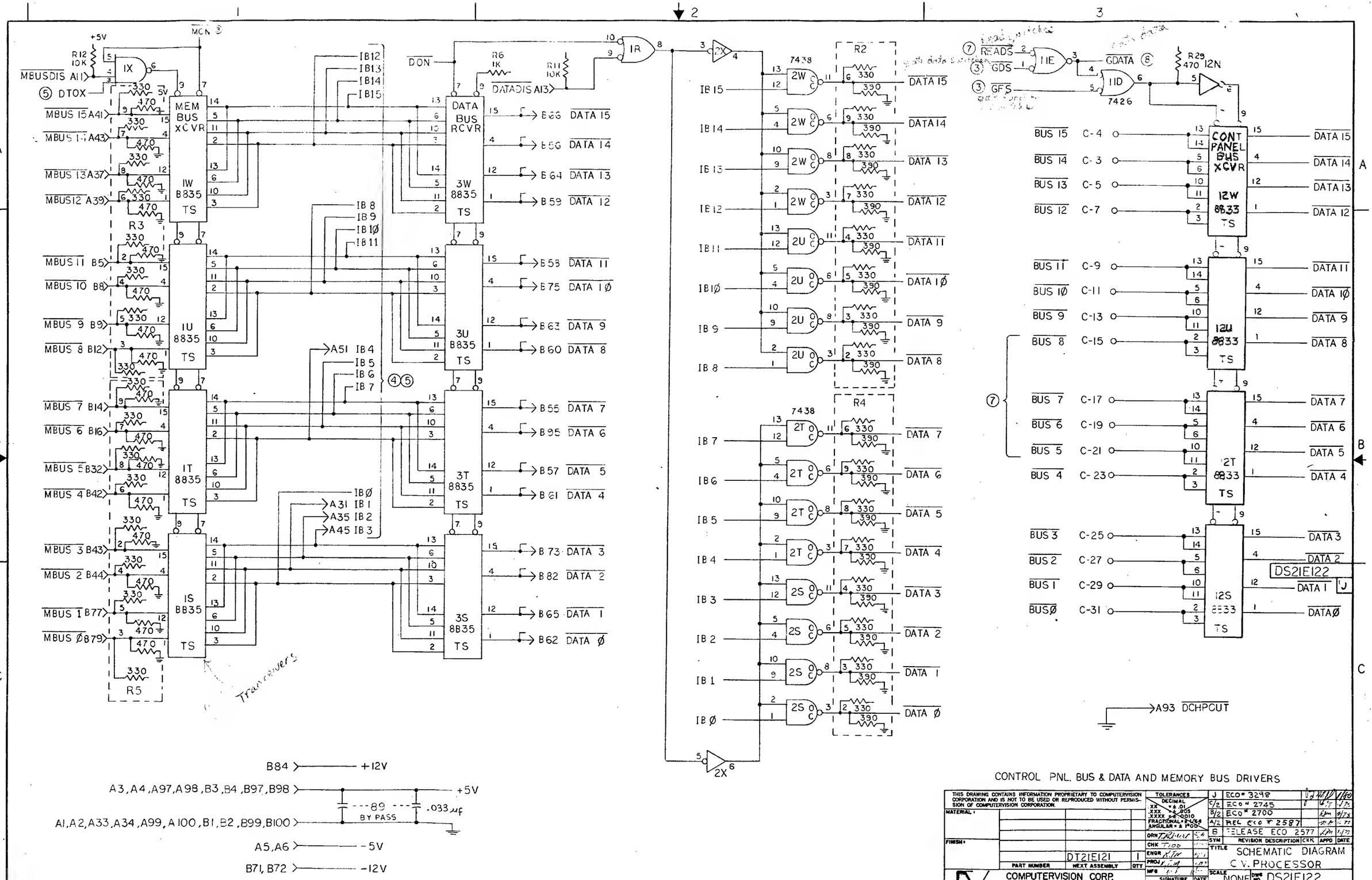
I/O Logic	7,9
Control Panel Encoding	7
Processor State Register	8
Control Panel Interface	8
Real Time Clock	9
Serial Line Control	10


RAD<0:7>
MULTIWAY BRANCH ROM
6: 1H
TST 0
TST 1
TST 2
TKB
CTZ
QROLI
SKIP
RAD <0:3>
SKIP LOGIC
3.8
SELD
SELB
ION
CSAVE
AZERO
CPUDEV
IR<0,8:9,13:15>
TEST MUX AND LOGIC
3
CONDITION LINES
TEST FIELD
ALU FIELD
RSC FIELD
CI FIELD
NAS FIELD
A FIELD
FM FIELD
B FIELD
CLK FIELD
DEC FIELD
LI FIELD
NA FIELD
IBS FIELD
ICF FIELD
ECF FIELD
MC FIELD
MA FIELD
SC FIELD
NEXT ADDRESS LOGIC
6: 2L.3L
IORST
INTA
MASKO
DATO(A.B.C)
DATI(A.B.C)
STRT
CLR
IOPLS
I/O CONTROL LINES
LDREG
SO
SI
FE
PUP
DEC2EN
DEC1EN
NEXT ADD-RESS ROM
6: 1K
TRUE
NAS 0
NAS 1
NAS 2
NAS 3
NAEN
CLOCK CONTROL ROM AND LOGIC
5: 10K. 11K. 12K
DTOX
CPUCLK
CPUCLK1
CPUCLK2
10MHZ
DC RESET
STOPCLK
MBUSY
ECF3
CCI
CCO
FASTDCH
I/O LOGIC
7: 1M.2M.2N.2P
IODT
IOP
CPUDEV
NA<0:7>
IR <5:15>
DECODE 1
DECODE 1, 2
DCHSYNC
INTRSYNC
RUNSYNC
IR<0:9,12>
IR<0:12>
DEC2EN
CPUDEV
EXI+SPDEV
ALCRYEN
MODE ROM LOGIC
6: 2R
IR <0.10:15>
INSTRUCTION REGISTER BUS <0:15>
LDIR
INSTRUCTION REGISTER
5: 3P. 4P.3R.4R
IB <1:4>
CPU COUNTER
5: 3P.4P.3R.4R
LCTR
CTEN
CTZ
I7
I6
I5
I4
I3
I2
I1
I0
CI
AF 3
AF 2
AF 1
AF 0
FM 0
FM 1
BF 3
BF 2
BF 1
BF 0
DEC 1
LDIBUF
RON
DON
MON
LDIR
IOP
IODT
DCHA
LDMAR
WRITE
READ
SCCC
SCC1
DE-CODE
3: 3C.4C. 5C.6L
SCC1
SCC0
IR7
IR8
IR9
ALU SHIFT-CARRY CONTROL ROM AND LOGIC
2: 5P.6P
ENACRY
SHFT1
SHFT2
CIN
A/B PORT LOGIC
2: 7R.8R.9R
A I
A 0
B 3
B 2
B 1
B 0
IR<1:4,67>
TO INTERNAL BUS
REGISTER AND ARITHMETIC-LOGIC UNIT (RALU)
4: 5S.5T.5U.5W
IO
QROLI
QLORI
ROLI
LORI
MSB
OV
LINK
2: 5X.6X
ALCCRY
C
Q
SCC1
SCC0
SHFT1
SHFT0
AZERO
ACRY
ALCCRY
LORI
ROLI
C
CARRY LOGIC
2.8
CSAVE
C
IR10
IR11
I4
ALCCRYEN
DATA-IN BUS <0:15>
FMO
AFO
AFI
IBUF MUX
APL
4
AON
IBUF
4
PSR AND MUX
8
PSON
CON <0:7>
INTERNAL BUS <0:15>
MEM TRANSCEIVERS
MON
MEMORY BUS <0:15>
DATA TRANSCEIVERS
DON
TO MCP
BUS BUS<0:15>
BUS TRANSCEIVERS
READ
GFS
GDS
SERIAL LINE CONTROL
9.10
RBUS13
RBUS14
RBUS15
RTC AND INTERFACE
9
DATA BUS <8:15>
DATA BUS <0:15>



CONTROL PNL. BUS & DATA AND MEMORY BUS DRIVERS

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J	ECO # 3298		
C/2	ECO # 2745		
B/2	ECO # 2700		
A/2	REL ECO # 2587		
B	RELEASE ECO 2577		
SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TOLERANCES: DECIMAL .XX = ± .01, .XXX = ± .005, .XXXX = ± .0010; FRACTIONAL = ± 1/64; ANGULAR = ± 1°00'

DRN T. Rivard; CHK T. Dodd; ENGR; PROJ; MFG; SIGNATURE; DATE

REMOVE ALL BURRS AND SHARP EDGES

PART NUMBER	NEXT ASSEMBLY	QTY
	DT21E121	1

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TITLE: SCHEMATIC DIAGRAM C.V. PROCESSOR

SCALE: NONE — DWG NO. DS21E122

UNIT WT. — SHEET 1 OF 10 SHEETS

Control Store RAMs

Control Store Register

A Port Logic

B Port Logic

Link

Shift from previous

Clock Control

8T98 8T97

PGØ RAD7 RAD6 RAD5 RAD4 RAD3 RAD2 RAD1 RADØ

8T97

CPUCLK 2

R17 1K

A 3K 6301 COO

B 5J COI

ALU 5H CO2

ALU RSC 4J CO3

CI MA 3H CO4

FM 5F CC CO5

SCF 4F CO6

6K SI74 — AF3 AF2 AF1 AFØ

SI74 6M — BF3 BF2 BF1 BFØ

6N SI74 — I7 I6 I5 I4 I3

6M — DECI

SI74 3E — WRITE READ R15-9

6F SI74 — FM1 FMØ CC1 CCØ SCCØ R15-7 CPUCLK1

6L S139 — PSON AON

FMØ 12N

5P 6301 SHIFT CONT ROM — ENACRY SHFT1 SHFTØ

ALCSHEN

SH MUX — I2 I1 IØ

6P 5156

IR8 IR9 IR7

10H 2X CIN

10M FORCE EFA

IG

LDMAR

DTOX 5E — B83 LDMAR

1D 2H — B85 WRITE MEM

1D — B45 READ MEM

R14-9 1K 4D ABSCYC

IOREQ

2H — B41 RQENB

7P ALCCRYEN ALCSHEN

DCHSYNC INTR SYNC RUN SYNC 5R

PG1 6H 8T98 PG1

ABORT CYC B48

IBUFSET

EXEC+DEFER

J IC LSIO7 K CLR CPUCLK 1

IR3 IR4+IR3 IR1 IR4 IR2 — 9R S253 — AI AØ

AF1 AFØ 9M 9M FMØ

R33 1K

IR1 9P BF3 IR6 — 8R S253 — B3 B2

BF2 9P IR2 BF2

IR4+IR3 IR6 IR3 IR4 8M — 7R S253 — BI BØ

BF1 IR7 IR4 IR4 BFØ

10M BF1

BFØ FM1 IRØ DECI 8P

IR11 1ON IR10 8P

ACRY ALCCRYEN 6R ACRY

1ON ALCCRYEN 7N S64 ALCCRY

ACRYSV DCHO 7D 2H — B39 OVFLO

SCCI SCCØ

MSB OV 4W

6X S253 TS — LORI QLORI IØ

ROLI

QLORI C 5X S253 TS — ROLI QROLI

LORI IØ 2X

DS21E122 J

MICRO INSTRUCTION WORD DECODE HIGH

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MATERIAL · FINISH ·

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES DECIMAL XX ± .01 XXX ± .005 XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00

DRN TMH 11/7/ CHK T.Mc 11/7/ ENGR PROJ MFG SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE SCHEMATIC DIAGRAM CV. PROCESSOR

SCALE NONE DWG NO. DS21E122

UNIT WT. SHEET 2 OF 10 SHEETS

COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803

Control Store Rams

Control Store Register

Test multiplexer

Load condition mux

Decoding controlled by ECF

Clear interrupts

Console function

Indicating results of test

SKIP Decode

CPUCLK 1 ⑤ — R15-9

ICF 3F CO7 — ECF 4H CO8 — ECF 4G IBC CO9 — PAGE 5G TEST CI0 — TEST 3G DECODE CI1 — NAS 3J CI2 — NA 5K CI3 — NA 4K CI4

3E S174 — 4E S174 — 6G S174 — 2G S174 — 2K S174 — 5L 2918 — 4L 2918

IBUFSET — LDIBUF ④ — ECF3 — R15-7

PG1 ② — PGØ ② — TST4 — TST3 — TST2 — TST1 — TSTØ ⑥ — DEC1 ②

NAS 3 — NAS 2 — NAS 1 — NAS Ø

CON7 ④⑥ — NA 7 — CON6 ④ — NA 6 ⑥ — CON5 ④ — NA 5 ⑥ — CON4 ④⑥ — NA 4

CON 3 ④⑥ — NA 3 — CON 2 ④⑥ — NA 2 — CON 1 ④⑥ — NA 1 — CONØ ④⑥ — NA Ø

PGØ — RA7 — RA6 — RA5 — RA4 — RA3 — RA2 — RA1 — RAØ — PG1

CPUCLK2 ⑤ — NAEN ⑥

BGC S138 — LCM ⑧ — DTOX ⑤

BFC S138 — LDIR ⑤ — LOADIR B7 — CTEN ⑤ — LCTR ⑤ — B30 DEFER — STC ⑧ Stepclock — DTOX ⑤

ECF4

LS138 5C — IOP ⑦⑦ — IODT — GDS ① — GFS ①⑧⑦ — ECF3 — DTOX ⑤

R13-7 470 — B86 FC3

R13-6 470 — B88 FC2

R13-9 470 — B91 FC1

R13-8 470 — B96 FCØ

T98

CION ⑧ — CCF ⑦ — LOAD CND ⑧

2H — B20 CLRINTEN

4C LS138 — B37 DCHI — B33 DCHØ ② — A60 DCHA

4D — R14-10 1K — B40 DCHDIS

8L S139 — RON ④ — DON ① — MON ①

CSAVE ⑧

IBUF1 IBUF2 IBUF3 IBUF4 IBUF5 IBUF6 IBUF7 IBUF8 IBUF9 IBUF10 IBUF11 ALCRYEN — 7X — ④

R14-2 1K — R14-3 1K — R14-5 1K

FSKP B80 — FBSY B78 — FBFRB B76 — 2K S174

TST2 — TST1 — TSTØ

R15-9 — ④ AZERØ — ⑤ CTZ — ① IBI2 — ⑦ CFUN — 2D S251 TS — R14-8 1K — TRUE ⑥ TO NA Rom

① IBØ — ① IB15 — ⑧ C — ⑤ IR5 — ⑤ IR7 — 2E S251 TS

R13-4 470 — R13-2 470 — DCHMØ B17 — DCHM1 B21

⑧② Q — ④ IBUF Ø — ⑤ IR Ø — 2F S251 TS

⑥ CPUDEV — IR8 ⑤ — R8-6 470 — ⑨ SELD A80 — ⑨ SELB A82 — R8-3 470 — ⑧ ION — 8N LS153

ACPWRFAIL AI4 — ⑨ — R8-5 470 — JP8

⑤ IR9 — 8M — 2K S174

⑤ IR14 — ⑤ IR13 — ④ AZERO — 7P — 7M — ⑤ IRØ — ⑤ IR15 — 8M — 7M — SKIP ⑥

IRØ ⑤

IF S139 — TBK 3 ⑥

⑥ FORCE RAD

MICRO INSTRUCTION ION WORD DECODE LOW

DS2IE122 J.

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MATERIAL — FINISH — PART NUMBER — NEXT ASSEMBLY — QTY

TOLERANCES DECIMAL XX ± .01 XXX ± .005 XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1 POS

DRN — CHK Tidd 11/17 — ENGR — PROJ — MFG — SIGNATURE — DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP. 300 SOUTH AVENUE BURLINGTON, MASS. 01803

SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE SCHEMATIC DIAGRAM CV. PROCESSOR

SCALE NONE — DWG NO. DS2IE122 — UNIT WT. — SHEET 3 OF 10 SHEETS

M-E MANAGEMENT S.A.M. 7881

Note Program to Load Roms

REGISTER/ARITHMETIC/LOGIC UNIT

5S AC21E119 Vcc PIN 10 GND PIN 30

5T AC21E119 Vcc PIN 10 GND PIN 30

5U AC21E119 Vcc PIN 10 GND PIN 30

5W AC21E119 Vcc PIN 10 GND PIN 30

7S SI75 · 7T SI75 · 7U SI75 · 7W SI75

9S 9T 9U 9W 10S 10T 10U 10W S253 TS

APL1 11S 6306 TS · APL2 11T 6306 TS · APL3 11U 6306 TS · APL4 11W 6306 TS

LOOK AHEAD CARRY 4U 74S182

DS21E122 J

APL ROM INTERNAL BUFFER AND RALU DATA PATHS

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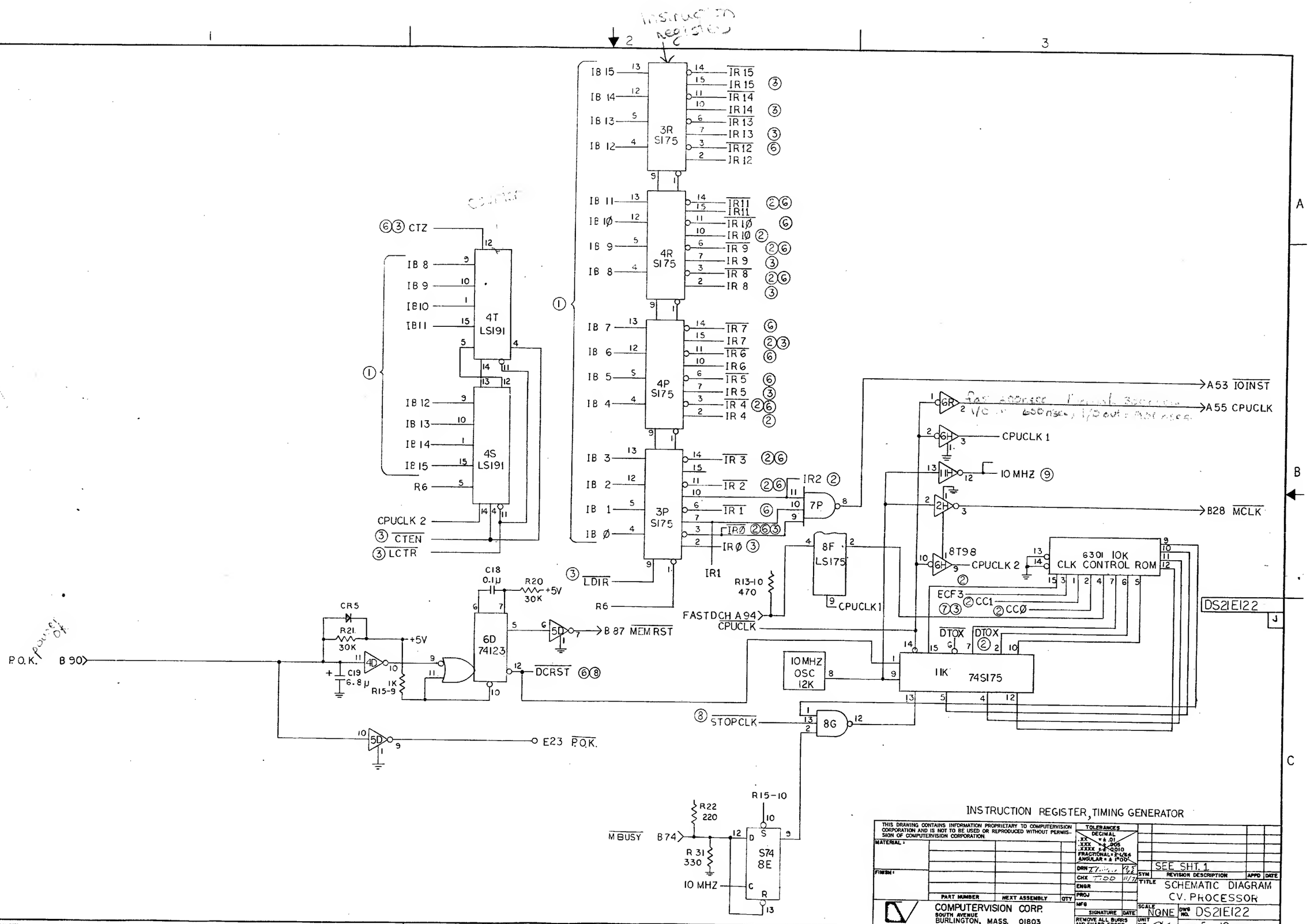
COMPUTERVISION CORP. 300TH AVENUE BURLINGTON, MASS. 01803

SEE SHT. 1

SCHEMATIC DIAGRAM CV. PROCESSOR

SCALE NONE · DWG NO. DS21E122 · SHEET 4 OF 10 SHEETS


INSTRUCTION REGISTER
IB 15
IB 14
IB 13
IB 12
3R SI75
IR 15
IR 15
IR 14
IR 14
IR 13
IR 13
IR 12
IR 12
IB 11
IB 10
IB 9
IB 8
4R SI75
IR11
IR11
IR 10
IR 10
IR 9
IR 9
IR 8
IR 8
IB 7
IB 6
IB 5
IB 4
4P SI75
IR 7
IR 7
IR 6
IR 6
IR 5
IR 5
IR 4
IR 4
IB 3
IB 2
IB 1
IB Ø
3P SI75
IR 3
IR 2
IR 1
IRØ
IRØ
IR1
IR2
7P
8F LS175
CPUCLK1
R13-10 470
FASTDCH A94
CPUCLK
3 LDIR
R6
3 CTEN
3 LCTR
CPUCLK 2
R6
IB 8
IB 9
IB10
IB11
4T LSI91
IB 12
IB 13
IB 14
IB 15
4S LSI91
63 CTZ
C18 0.1µ
R20 30K +5V
CR5
R21 30K
+5V
C19 6.8µ
1K R15-9
6D 74123
5D
B 87 MEMRST
DCRST 68
P.O.K.
B 90
5D
E23 P.O.K.
A53 IOINST
A55 CPUCLK
6R
CPUCLK 1
6H
10 MHZ 9
11H
2H
B28 MCLK
8T98
CPUCLK 2
6301 10K CLK CONTROL ROM
ECF3
2 CC1
2 CCØ
DS21E122
DTOX
DTOX
11K 74S175
10MHZ OSC 12K
8 STOPCLK
8G
R15-10
R22 220
MBUSY
B74
R 31 330
10 MHZ
S74 8E
INSTRUCTION REGISTER, TIMING GENERATOR
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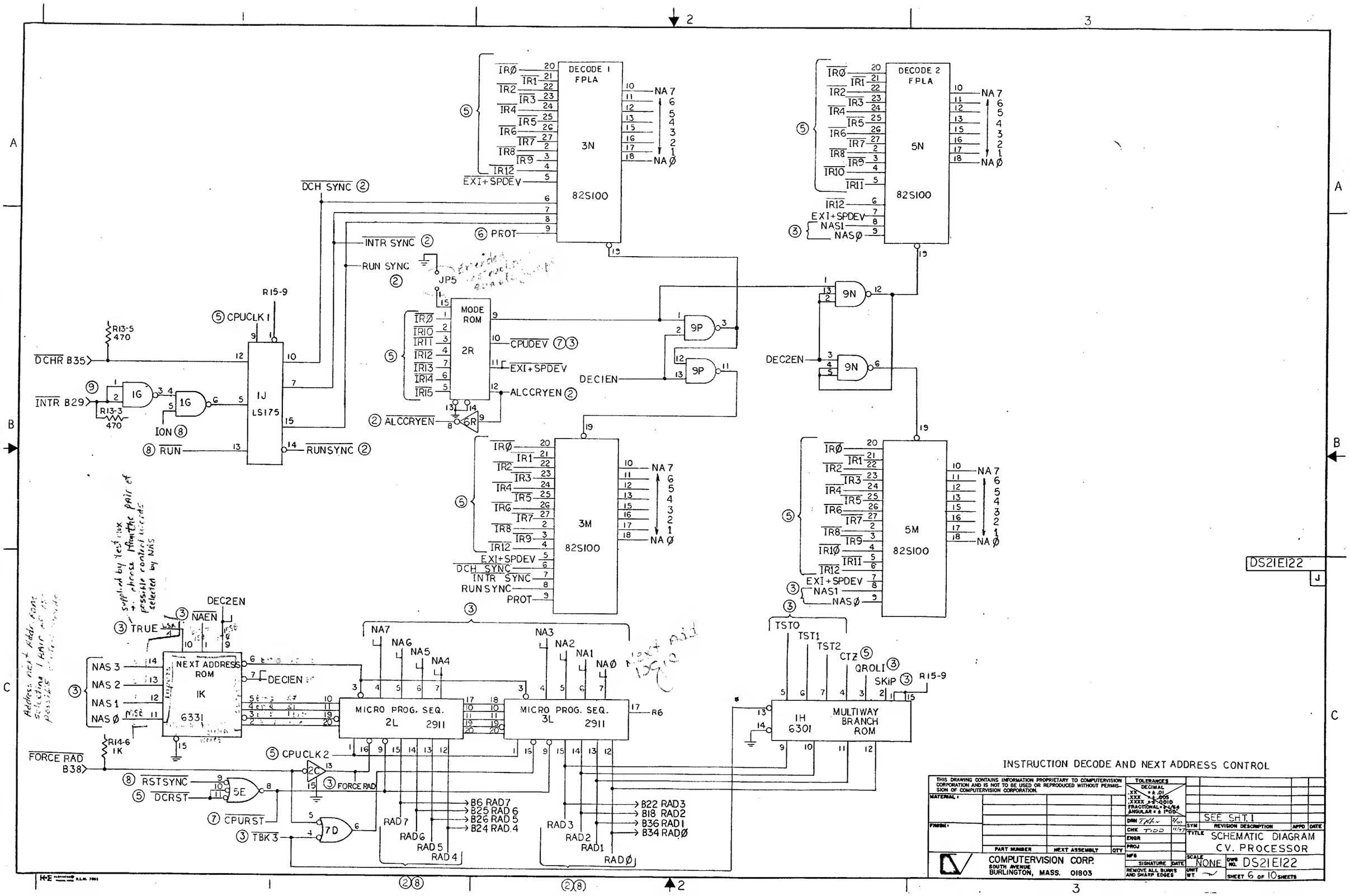
MATERIAL
FINISH
PART NUMBER
NEXT ASSEMBLY
QTY
TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SHT. 1
SYM
REVISION DESCRIPTION
APPD
DATE
TITLE
SCHEMATIC DIAGRAM
CV. PROCESSOR
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
SCALE NONE
DWG NO. DS21E122
UNIT WT.
SHEET 5 OF 10 SHEETS



DS21E122 J

INSTRUCTION DECODE AND NEXT ADDRESS CONTROL

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TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1° MAT'L ± % FINISH

DRN TMH 9/87 CHK TDD 11/87 ENGR PROJ MFG

PART NUMBER	NEXT ASSEMBLY	QTY

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	APPD	DATE

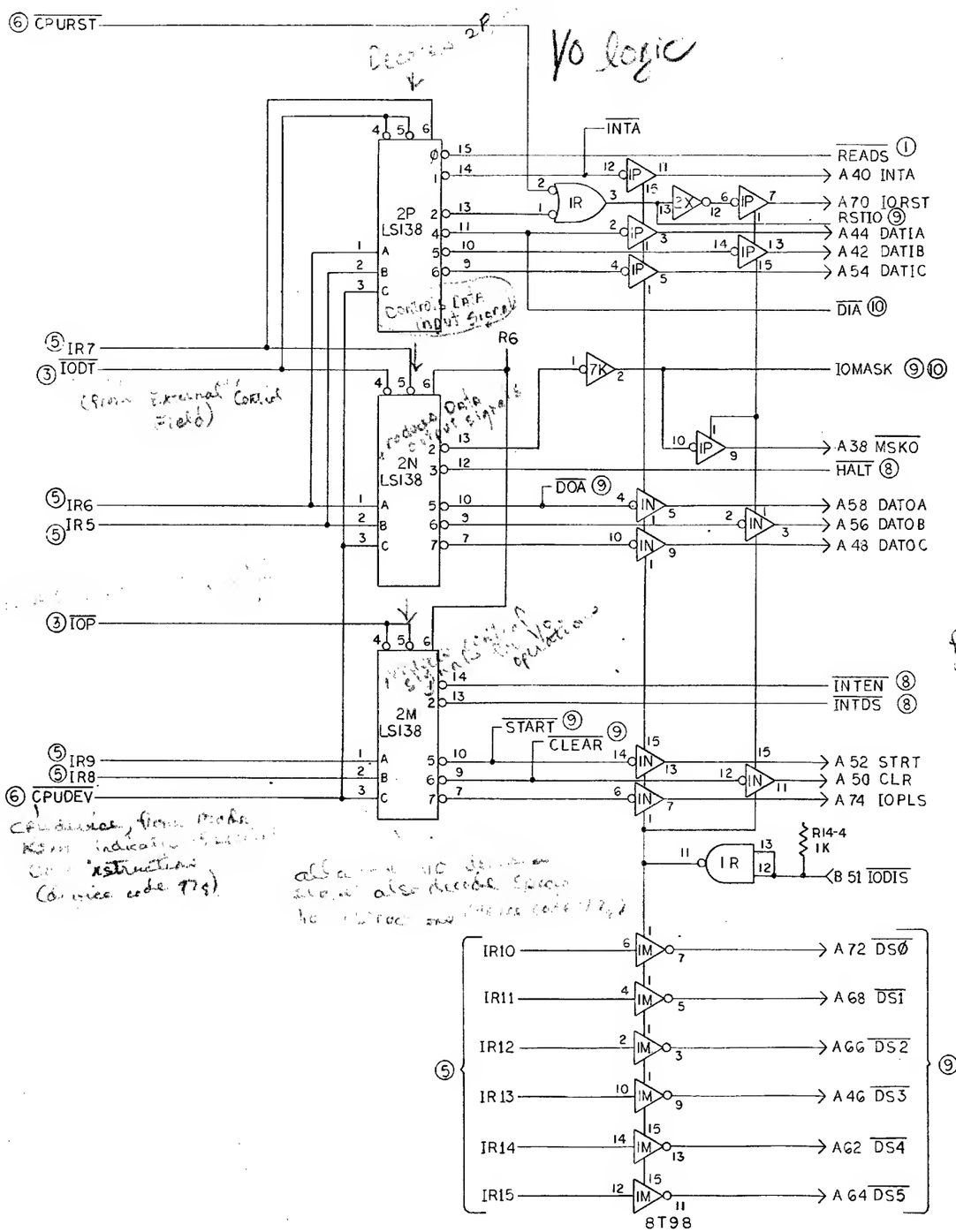
SEE SHT. 1

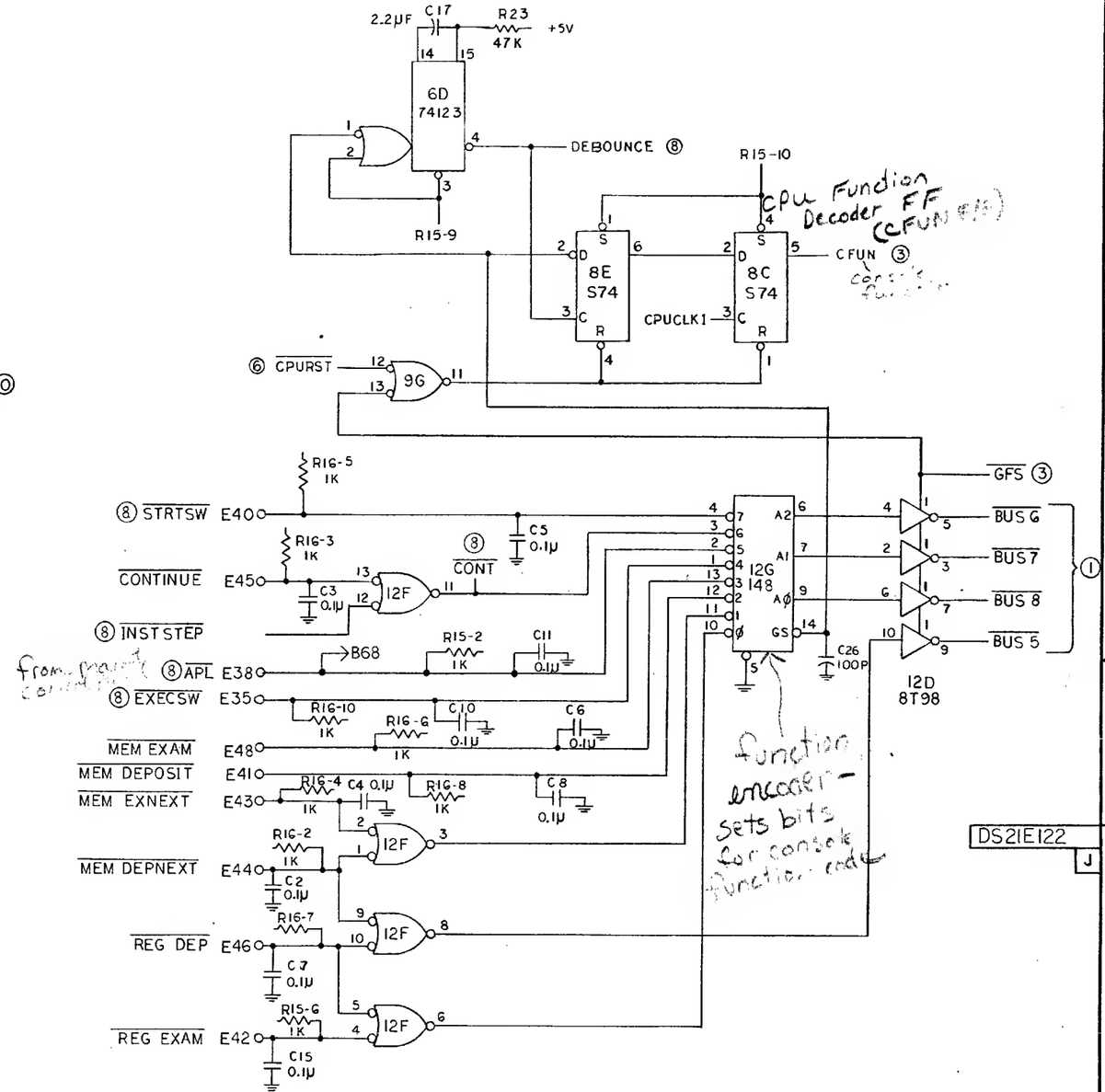
TITLE SCHEMATIC DIAGRAM CV. PROCESSOR

COMPUTERVISION CORP. SOUTH AVENUE BURLINGTON, MASS. 01803

SCALE NONE DWG NO. DS21E122

UNIT WT. SHEET 6 OF 10 SHEETS





CONTROL PANEL FUNCTION ENCODE I/O PULSE GENERATOR

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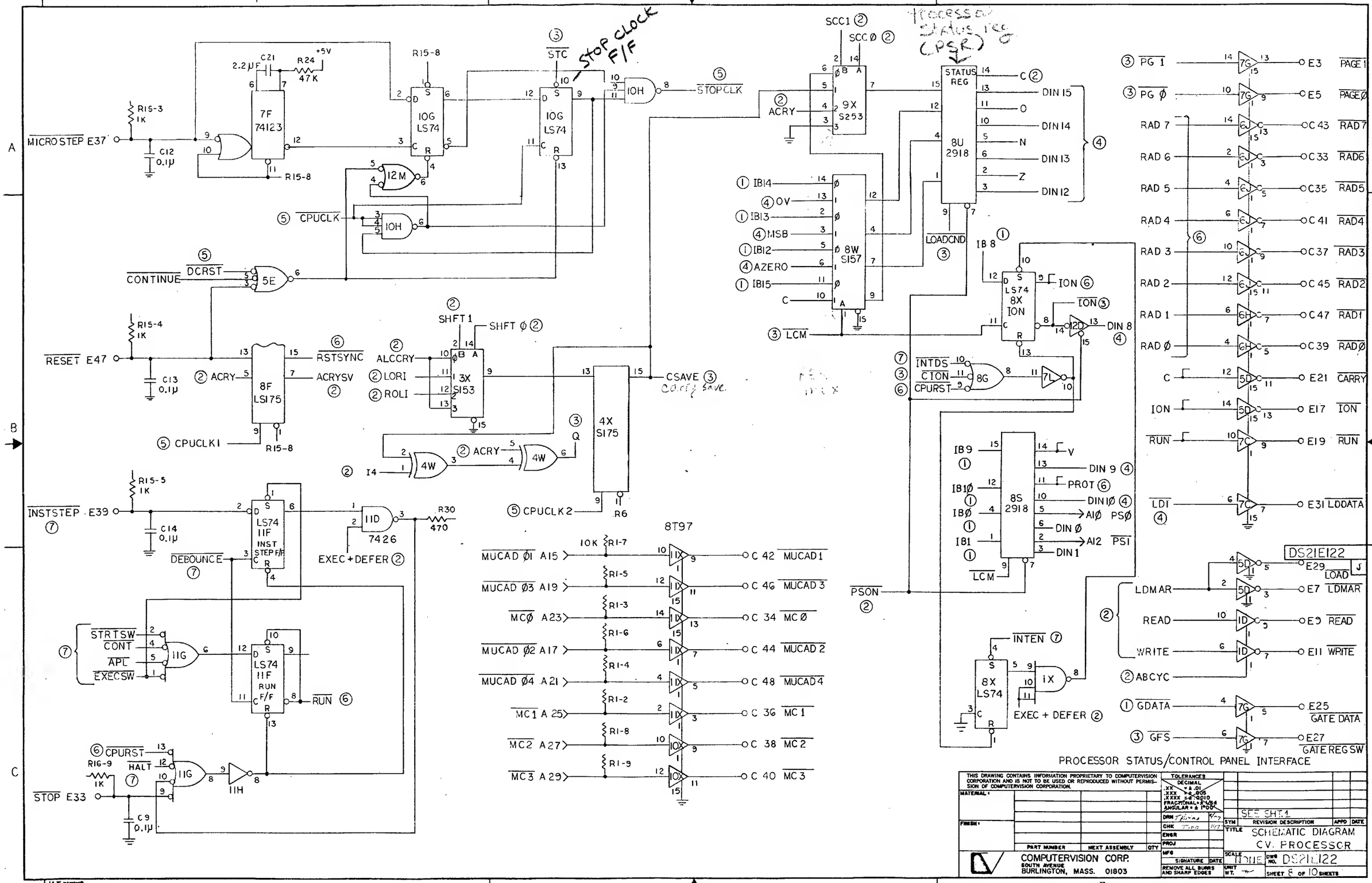
MATERIAL	
FINISH	
PART NUMBER / NEXT ASSEMBLY / QTY	
TOLERANCES DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010; FRACTIONAL ± 1/64; ANGULAR ± 1° 00'	
DRN	
CHK TJD	1/71
ENGR	
PROJ	
MFG	
SIGNATURE / DATE	
REMOVE ALL BURRS AND SHARP EDGES	
SCALE	NONE
UNIT WT.	
SIZE	D
DWG NO.	DS21E122
SHEET	7 OF 10 SHEETS

SEE SHT.1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: SCHEMATIC DIAGRAM CV. PROCESSOR

COMPUTERVISION CORP. 8 SOUTH AVENUE BURLINGTON, MASS. 01803



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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

DRN | CHK | ENGR | PROJ | MFG

SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

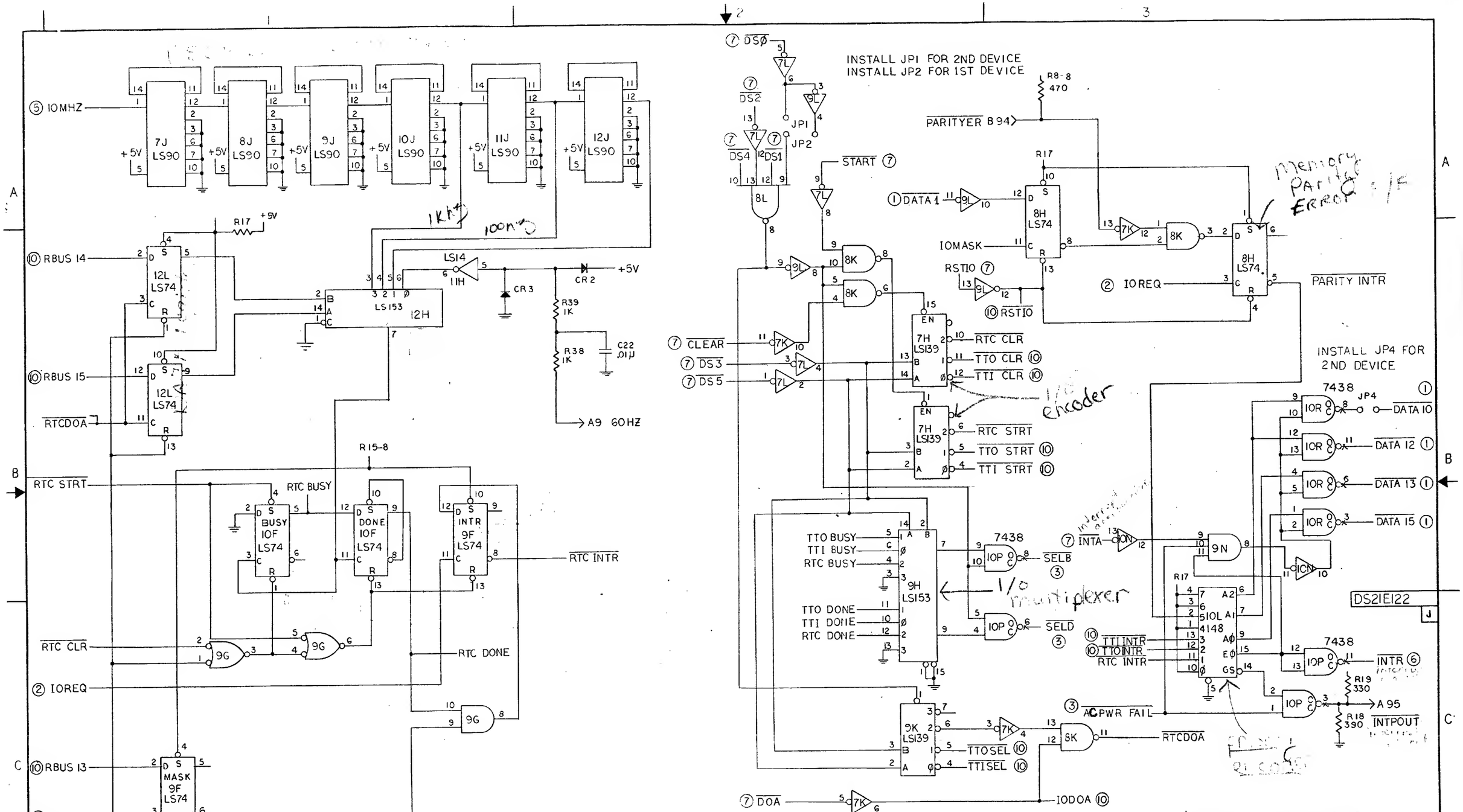
SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: SCHEMATIC DIAGRAM
CV PROCESSOR

SCALE: NONE | DWG NO. DS21E122

UNIT WT. | SHEET 8 OF 10 SHEETS



I/O LOGIC AND REAL TIME CLOCK

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

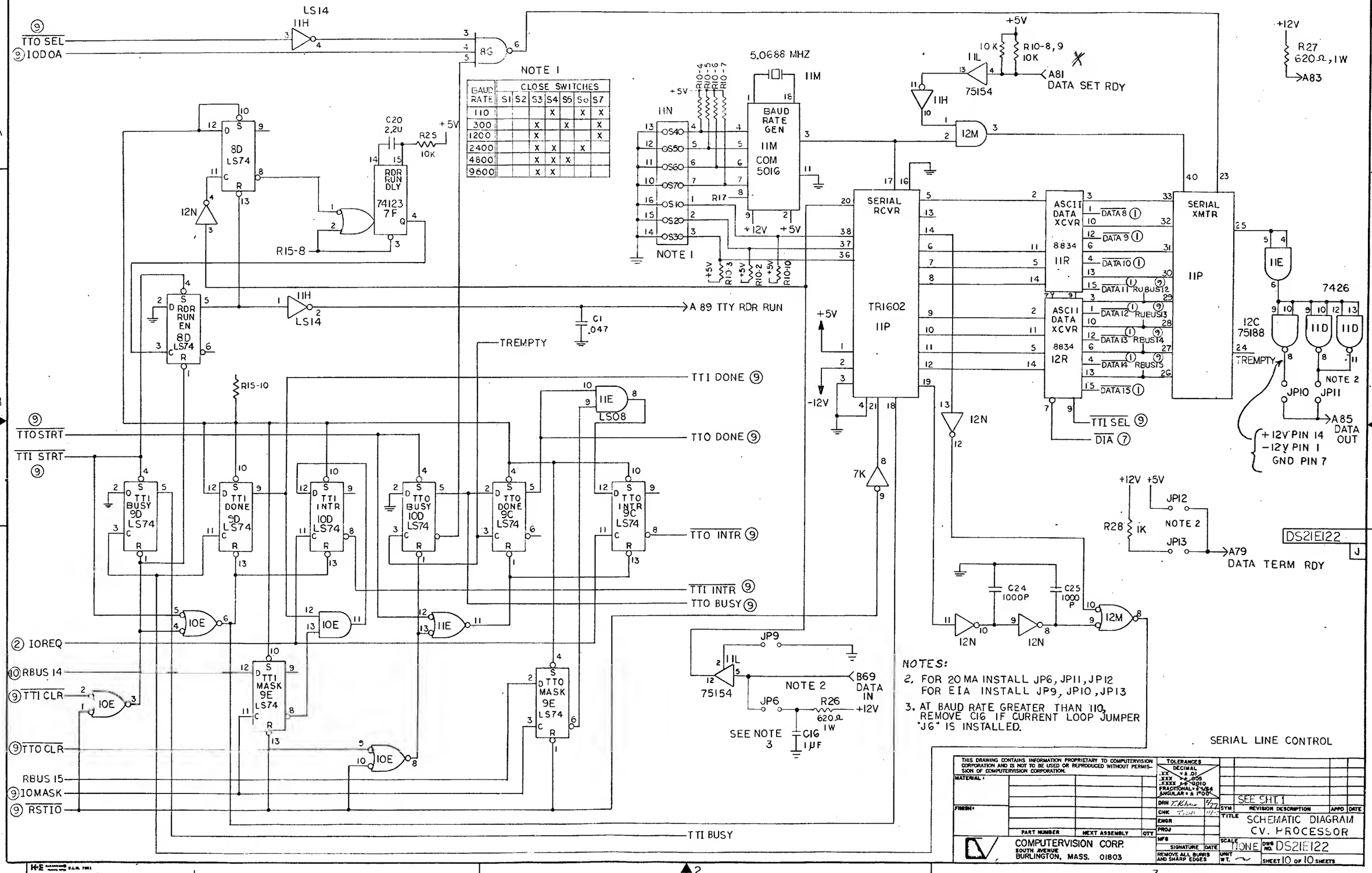
DRN T. Kh... 1/71
CHK T. ... 1/71
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE SCHEMATIC DIAGRAM CV. PROCESSOR

SCALE NONE
DWG NO. DS21E122
UNIT WT.
SHEET 9 OF 10 SHEETS



NOTE 1

BAUD RATE	CLOSE SWITCHES S1	S2	S3	S4	S5	S6	S7
110				X		X	X
300			X		X		X
1200			X				X
2400			X	X		X	
4800			X	X	X		
9600			X	X			

NOTES:

2. FOR 20 MA INSTALL JP6, JP11, JP12
   FOR EIA INSTALL JP9, JP10, JP13
3. AT BAUD RATE GREATER THAN 110, REMOVE C16 IF CURRENT LOOP JUMPER "J6" IS INSTALLED.

SERIAL LINE CONTROL

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MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN T. Kohn 2/77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

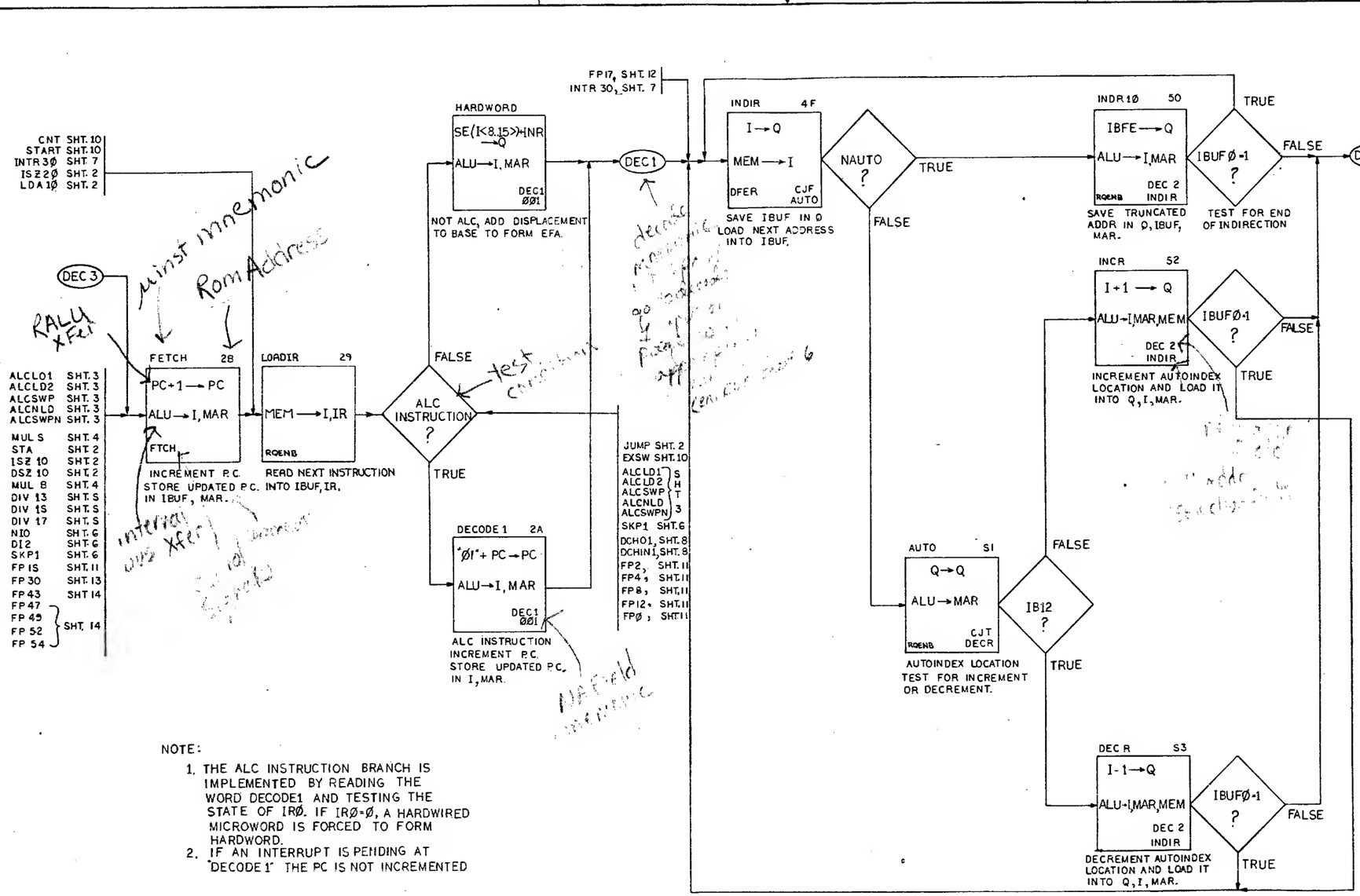
SYM | REVISION DESCRIPTION | APPD | DATE
SEE SHT. 1

TITLE SCHEMATIC DIAGRAM CV. PROCESSOR

SCALE NONE
DWG NO. DS21E122
UNIT WT.
SHEET 10 OF 10 SHEETS

Microprogram Flow Chart

	Sheet No.
Instruction Fetch	1
Indirect Addressing	1
Move Data Instructions	2
Modify Memory Instructions	2
Jump Instructions	2
Arithmetic/Logic Instructions	3
Unsigned Integer Multiplication	4
Unsigned Integer Division	5
I/O Instructions	6
Interrupts	7
Data Channels	8
Pseudo-Instructions	9
Console Functions	9,10
Floating Point Interface	11-14
Microdiagnostics	15-27


CNT SHT. 10
START SHT. 10
INTR 30 SHT. 7
ISZ 20 SHT. 2
LDA 10 SHT. 2
DEC 3
RALU XFer
ALCLO1 SHT. 3
ALCLD2 SHT. 3
ALCSWP SHT. 3
ALCNLD SHT. 3
ALCSWPN SHT. 3
MUL S SHT. 4
STA SHT. 2
ISZ 10 SHT. 2
DSZ 10 SHT. 2
MUL B SHT. 4
DIV 13 SHT. S
DIV 15 SHT. S
DIV 17 SHT. S
NIO SHT. 6
DI2 SHT. 6
SKP1 SHT. 6
FP 15 SHT. 11
FP 30 SHT. 13
FP 43 SHT 14
FP 47
FP 49
FP 52 SHT. 14
FP 54
FETCH 28
PC+1 → PC
ALU → I, MAR
FTCH
INCREMENT P.C.
STORE UPDATED P.C. IN IBUF, MAR.
LOADIR 29
MEM → I, IR
ROENB
READ NEXT INSTRUCTION INTO IBUF, IR.
ALC INSTRUCTION ?
FALSE
TRUE
HARDWORD
SE(I<8,15>)+NR → Q
ALU → I, MAR
DEC1 ØØ1
NOT ALC, ADD DISPLACEMENT TO BASE TO FORM EFA.
DECODE 1 2A
"Ø1" + PC → PC
ALU → I, MAR
DEC1 ØØ1
ALC INSTRUCTION INCREMENT P.C. STORE UPDATED P.C. IN I, MAR.
DEC1
FP17, SHT. 12
INTR 30, SHT. 7
JUMP SHT. 2
EXSW SHT. 10
ALCLD1
ALCLD2
ALCSWP
ALCNLD
ALCSWPN
SHT. 3
SKP1 SHT. 6
DCH01, SHT. 8
DCHINI, SHT. 8
FP2, SHT. 11
FP4, SHT. 11
FP8, SHT. 11
FP12, SHT. 11
FPØ, SHT. 11
INDIR 4F
I → Q
MEM → I
DFER
CJF AUTO
SAVE IBUF IN Q LOAD NEXT ADDRESS INTO IBUF.
NAUTO ?
TRUE
FALSE
INDR 10 50
IBFE → Q
ALU → I, MAR
DEC 2 INDIR
ROENB
SAVE TRUNCATED ADDR IN Q, IBUF, MAR.
IBUFØ=1 ?
TRUE
FALSE
TEST FOR END OF INDIRECTION
DEC 2
INCR 52
I+1 → Q
ALU → I, MAR, MEM
DEC 2 INDIR
INCREMENT AUTOINDEX LOCATION AND LOAD IT INTO Q, I, MAR.
IBUFØ=1 ?
FALSE
TRUE
AUTO S1
Q → Q
ALU → MAR
CJT DECR
ROENB
AUTOINDEX LOCATION TEST FOR INCREMENT OR DECREMENT.
IB12 ?
FALSE
TRUE
DEC R S3
I-1 → Q
ALU → I, MAR, MEM
DEC 2 INDIR
DECREMENT AUTOINDEX LOCATION AND LOAD IT INTO Q, I, MAR.
IBUFØ=1 ?
FALSE
TRUE
decode - at decode time CPU evaluates IR bits in order to execute instruction determines which RAD will follow previous RAD
NOTE:
1. THE ALC INSTRUCTION BRANCH IS IMPLEMENTED BY READING THE WORD DECODE1 AND TESTING THE STATE OF IRØ. IF IRØ=Ø, A HARDWIRED MICROWORD IS FORCED TO FORM HARDWORD.
2. IF AN INTERRUPT IS PENDING AT "DECODE 1" THE PC IS NOT INCREMENTED
INSTRUCTION FETCH
INDIRECT ADDRESSING
DS21E015
E
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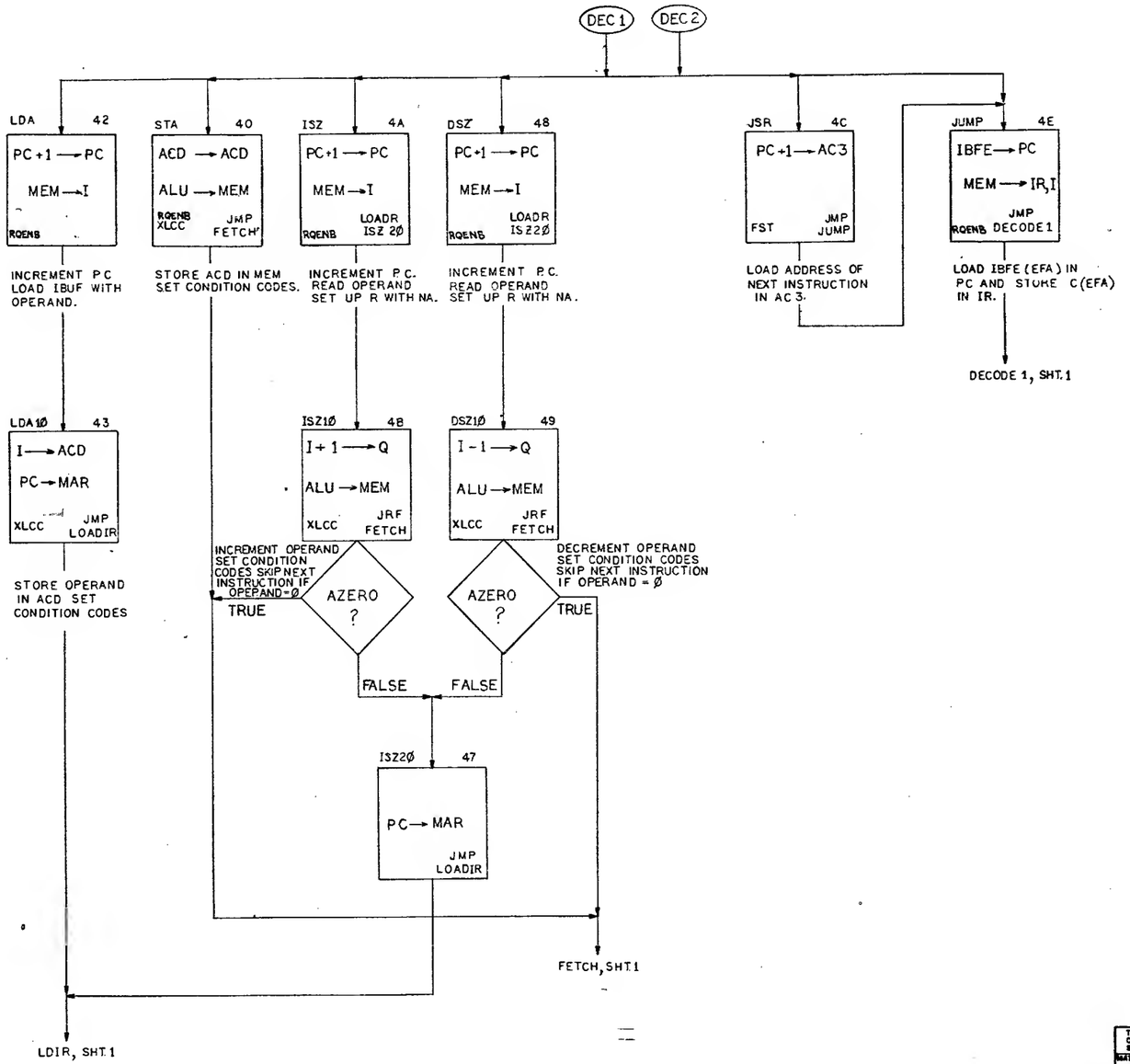
E ECO # 3433
D ECO # 3258
B ECO # 2779
A RELEASE ECO 2571
CVP MICROPROGRAM FLOW CHARTS
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
NONE
DS21E015
SHEET 1 OF 27



MOVE DATA MODIFY MEMORY AND JUMP INSTRUCTIONS

DS21E015
E

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MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN TR 3-11-77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

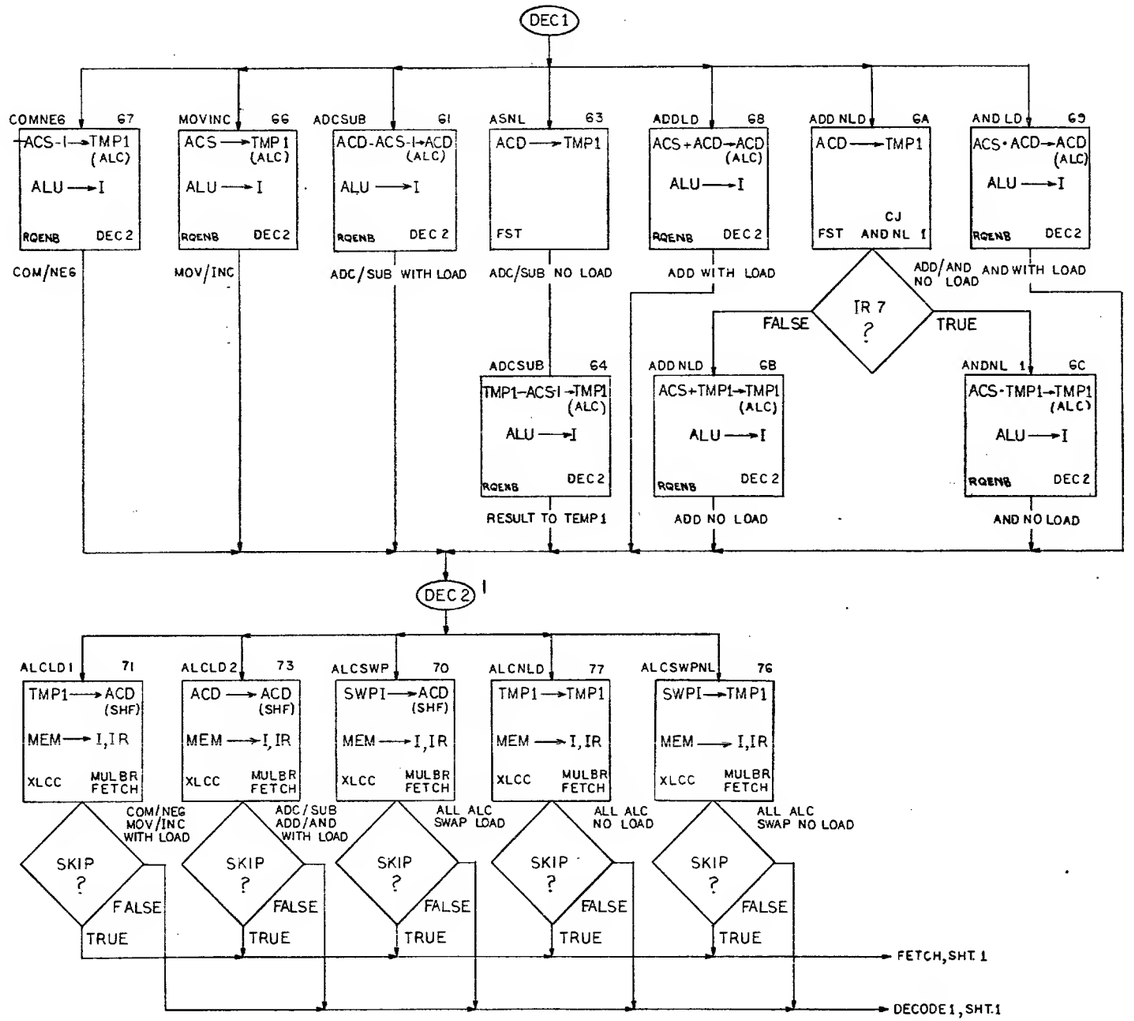
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SEE SHT 1

SYM | REVISION DESCRIPTION | APPD | DATE

TITLE: CVP MICROPROGRAM FLOW CHARTS

SCALE: NONE
SIZE: E
DWG NO. DS21E015
SHEET 2 OF 27



DS21E015
E

ALC INSTRUCTIONS

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MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN T. Bivens 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1
SYM | REVISION DESCRIPTION | APPD | DATE

TITLE CVP MICROPROGRAM FLOW CHARTS

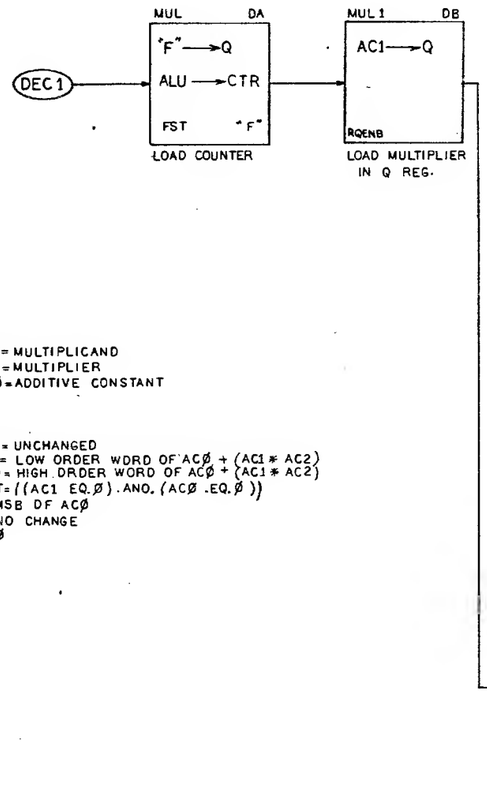
SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 3 OF 27 SHEETS

INPUT:

AC2 = MULTIPLICAND
AC1 = MULTIPLIER
ACØ = ADDITIVE CONSTANT

OUTPUT:

AC2 = UNCHANGED
AC1 = LOW ORDER WORD OF ACØ + (AC1 * AC2)
ACØ = HIGH ORDER WORD OF ACØ + (AC1 * AC2)
ZBIT = ((AC1 EQ.Ø) .ANO. (ACØ .EQ.Ø))
N = MSB OF ACØ
C = NO CHANGE
O = Ø



DS21E015
E

UNSIGNED INTEGER MULTIPLICATION

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

DRN T. Rivera 3/77
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

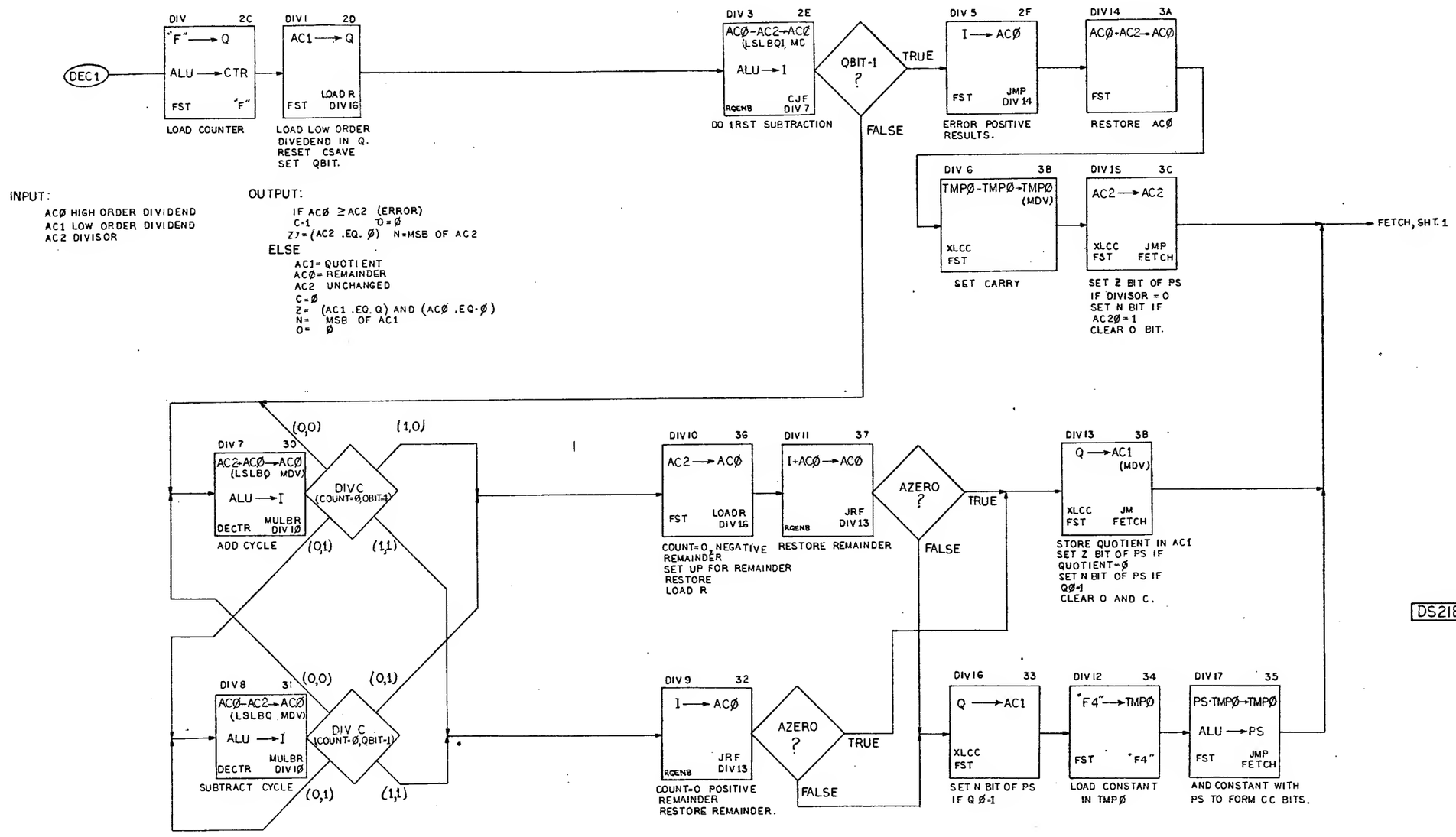
TITLE CVP MICROPROGRAM FLOW CHARTS

SCALE NONE | DWG NO. DS21E015 | REV E

UNIT WT.

SHEET 4 OF 27 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



UNSIGNED INTEGER DIVISION

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MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN T. Rabine 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SEE SHT. 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 5 OF 27 SHEETS

DEC 1

DI 84
DATA → I
IODT IOIN JMP DI1
DI A,B,C READS,INTA

DO 8E
ACD → DATA
IOUT IOUT
DOA,B,C MSKO, HALT, NIO, INTEN, INTDS

001 8F
ACD → ACD
XLCC FST JMP DI2
SET CONDITION CODE

SKP 80
PC+1 → PC
ALU → I, MAR
RQENB FCTH
SKPBN SKPBZ SKPDN SKPDZ

81
MEM → I, IR
MULBR FETCH

SKIP ?
FALSE → OECODE 1, SHT. 1
TRUE

DI1 86
I → ACD
XLCC FST
LOAD DATA IN ACD
SET CONDITION CODE

IORST 85
IODT IOIN JMP DI2
IORST

DI2 87
RQENB IOP IOIN JMP FETCH
(CONTROL FUNCTION, IF ANY)

FETCH, SHT. 1

CONDITION CODE BITS FOR I/O

	IORST SKP	DIA,B,C READS INTA	DOA,B,C MSKO HALT NIO INTEN INTDS
C	NO CHANGE	NO CHANGE	NO CHANGE
O	NO CHANGE	Ø	Ø
N	NO CHANGE	MSB DATA IN	MSB DATA OUT
Z	NO CHANGE	DATA IN = Ø	DATA OUT = Ø

DSE21E015
E

I/O INSTRUCTIONS

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

DRN 9/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

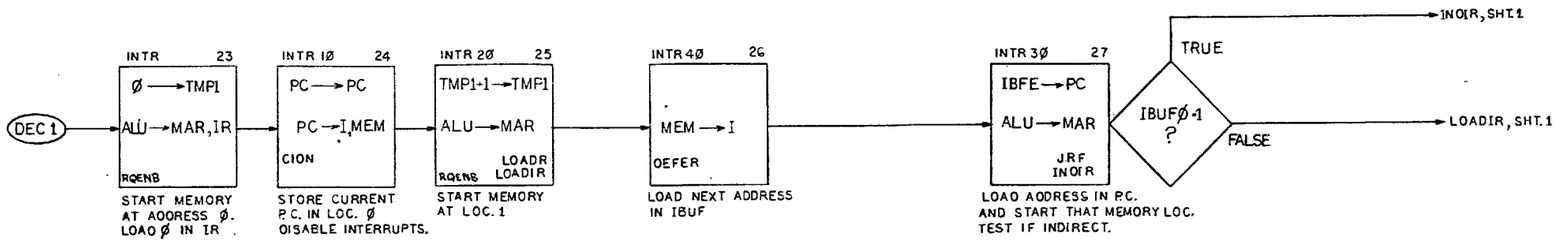
SEE SHT. 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHART

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SCALE NONE
DWG NO. DSE1E015
SHEET WT.
SHEET 6 OF 27 SHEETS



DS21E015
E

INTERRUPT

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MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN T. Kiss 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

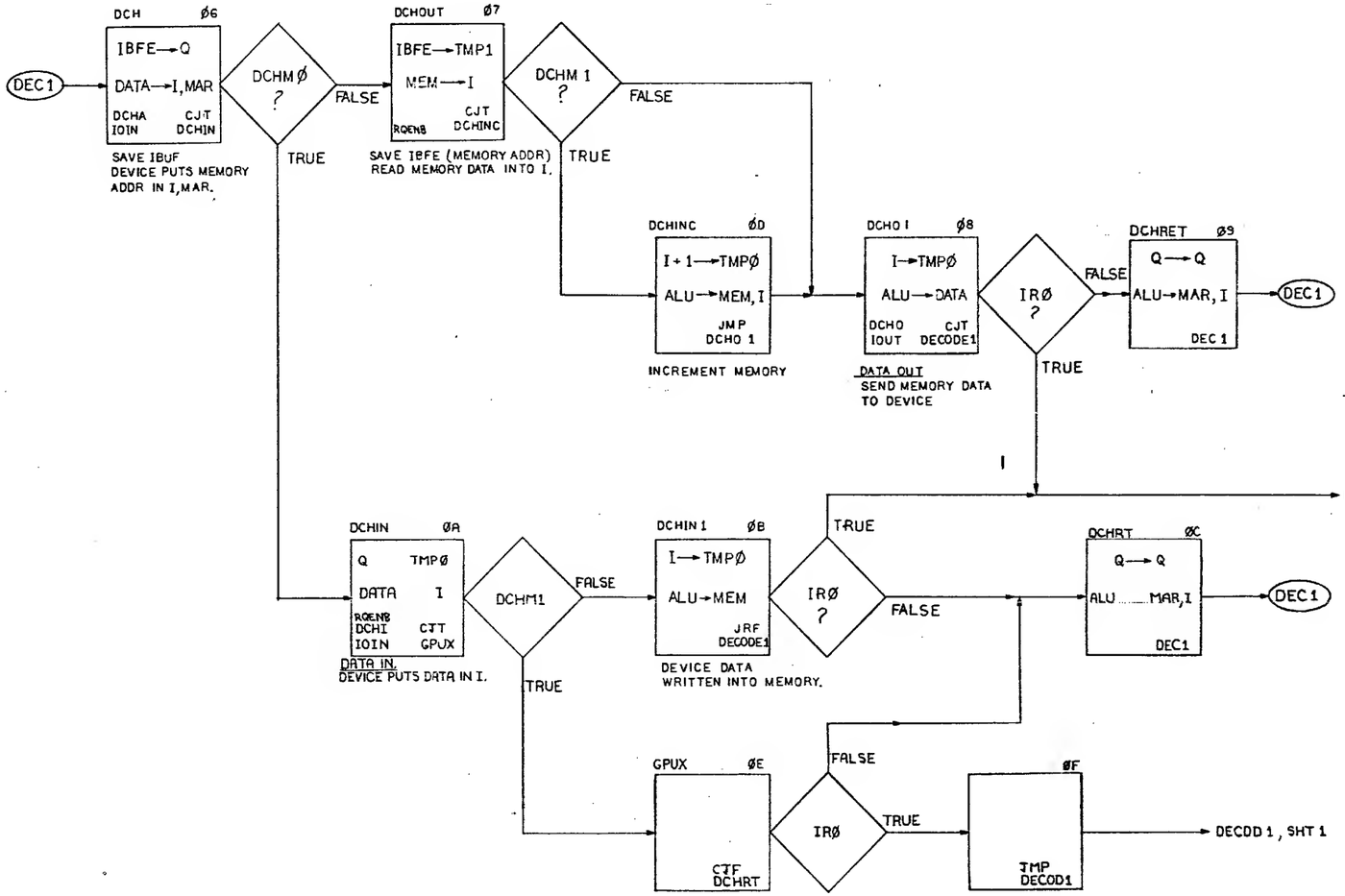
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE
DWG NO. DS21E015
UNIT WT. —
SHEET 7 OF 27 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

FUNCTION	DCHMØ	DCHM 1
DATA OUT	Ø	Ø
INCREMENT MEMORY	Ø	1
DATA IN	1	Ø
GPU TRANSFER	1	1



DS21E015
E

DATA CHANNEL

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MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°

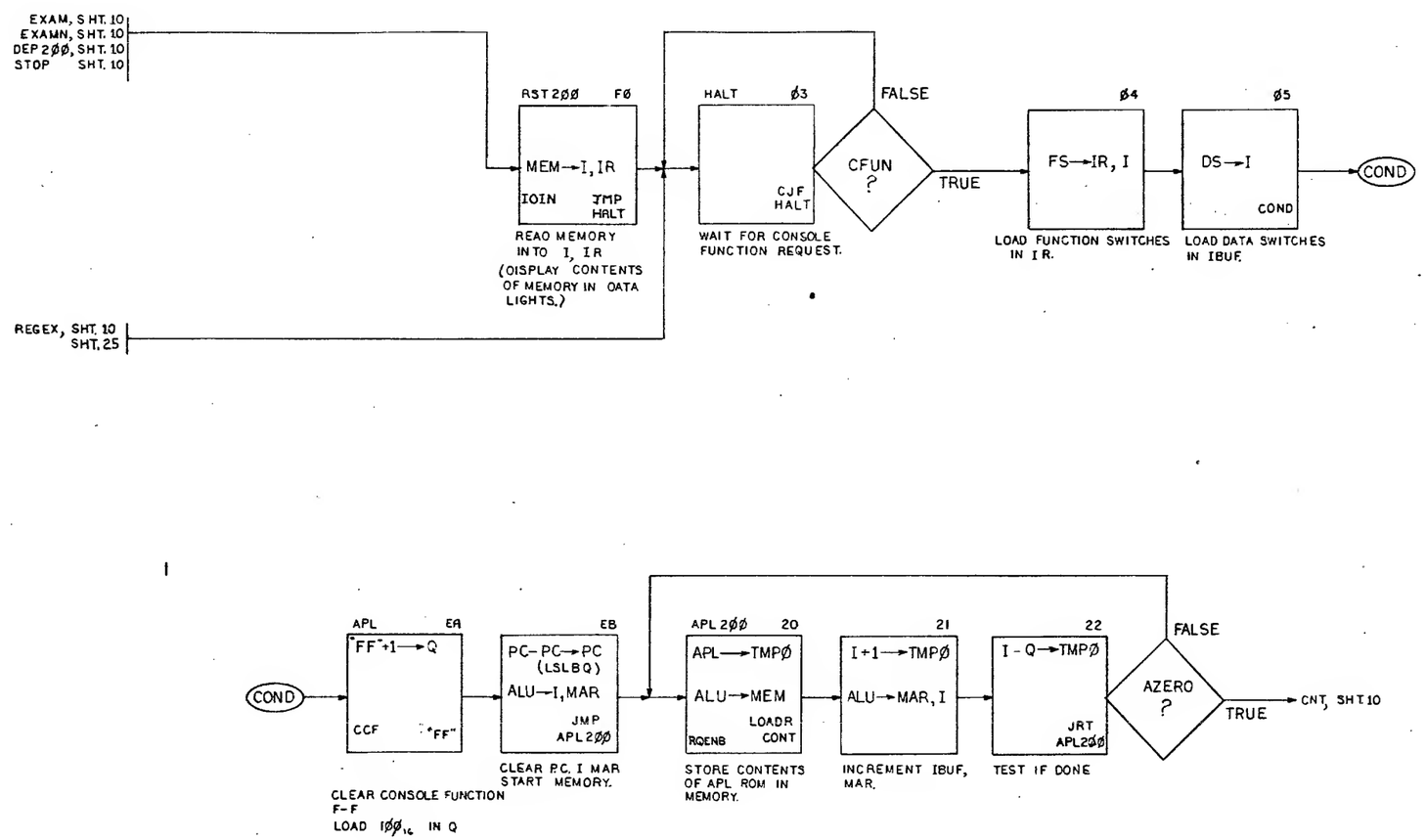
DRN T.Richard 9/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT. 1		

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 8 OF 27 SHEETS



DS21E015
E

CONSOLE FUCNCTIONS I
(RESET, HALT STATE, APL)

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

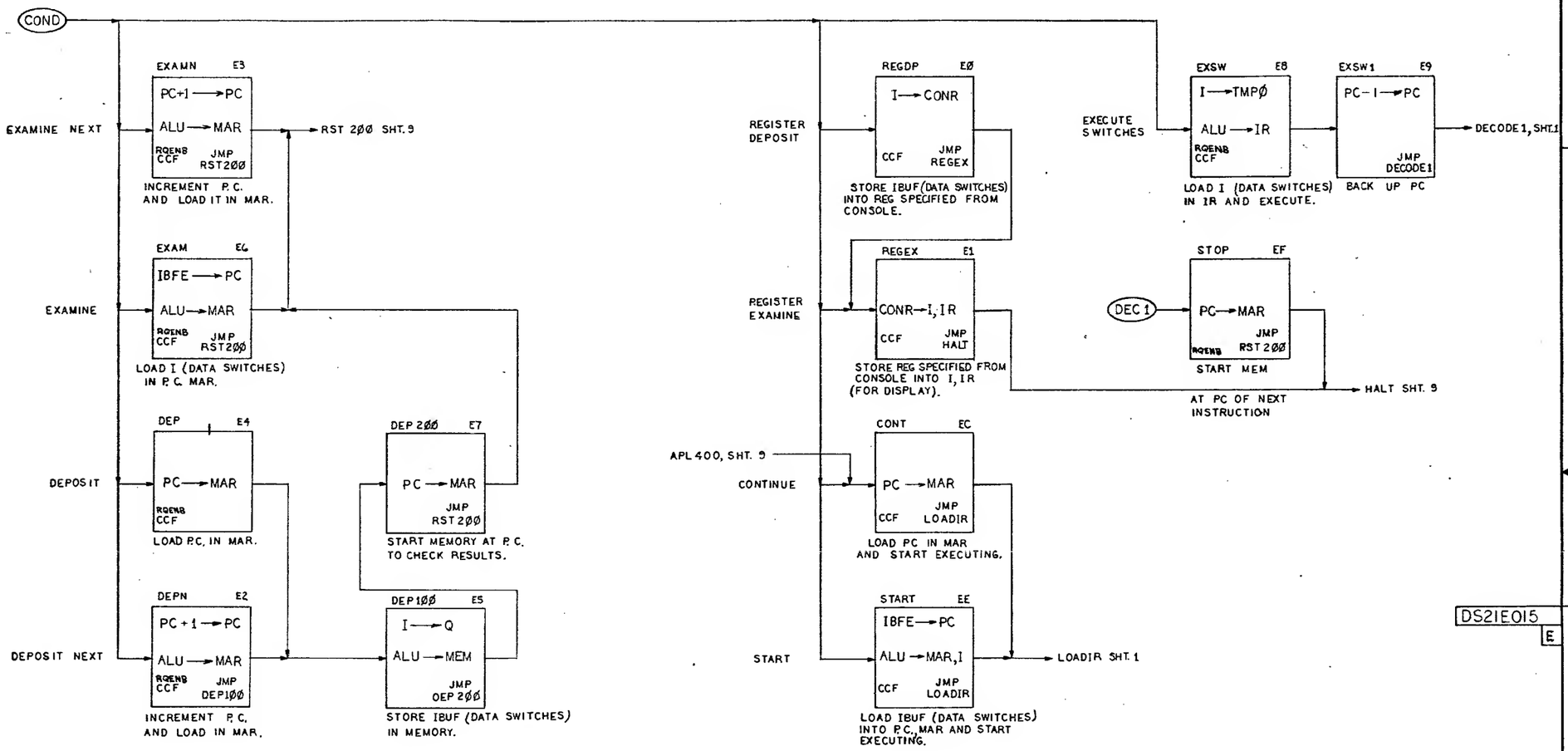
TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN T. Palmer 4/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1
SYM | REVISION DESCRIPTION | APPD | DATE

TITLE CVP MICROPROMGRAM FLOW CHART
SCALE NONE
DWG NO. DS21E015
UNIT WT. —
SHEET 9 OF 27 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



DS2IE015
E

CONSOLE FUNCTIONS II

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

TOLERANCES	
DECIMAL	
.XX	±0.01
.XXX	±0.005
.XXXX	±0.0010
FRACTIONAL	±1/64
ANGULAR	±0 MOD.

DRN T. Klein 11/12
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

MATERIAL
FINISH

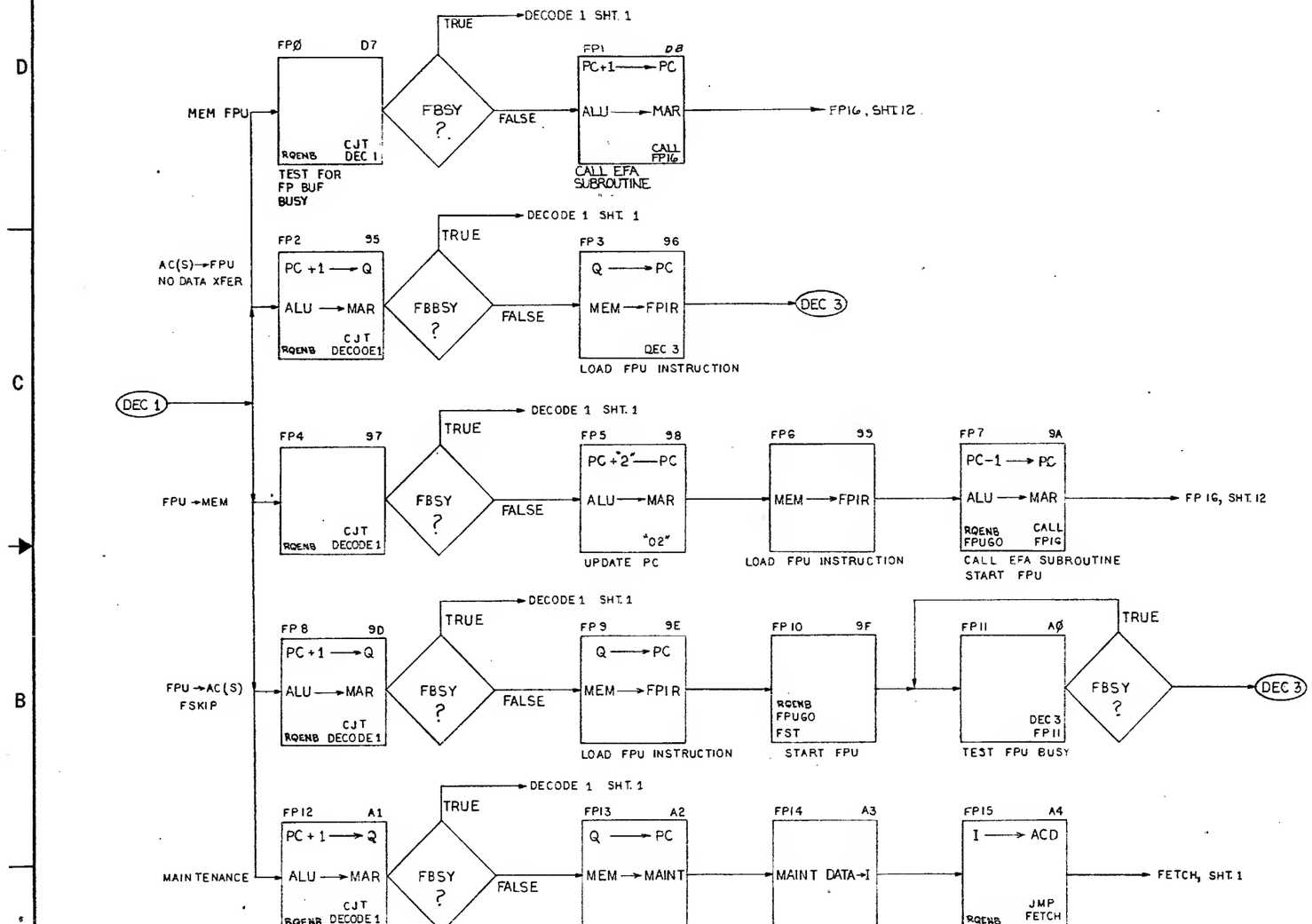
PART NUMBER	NEXT ASSEMBLY	QTY

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT. 1		

TITLE: CVP MICROPROGRAM FLOW CHART

SCALE: NONE
DWG NO. DS2IE015
UNIT WT.
SHEET 10 OF 27 SHEETS



DS21E015
E

FLOATING POINT INTERFACE
(ENTRY POINTS)

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN J.Ribeiro 5/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

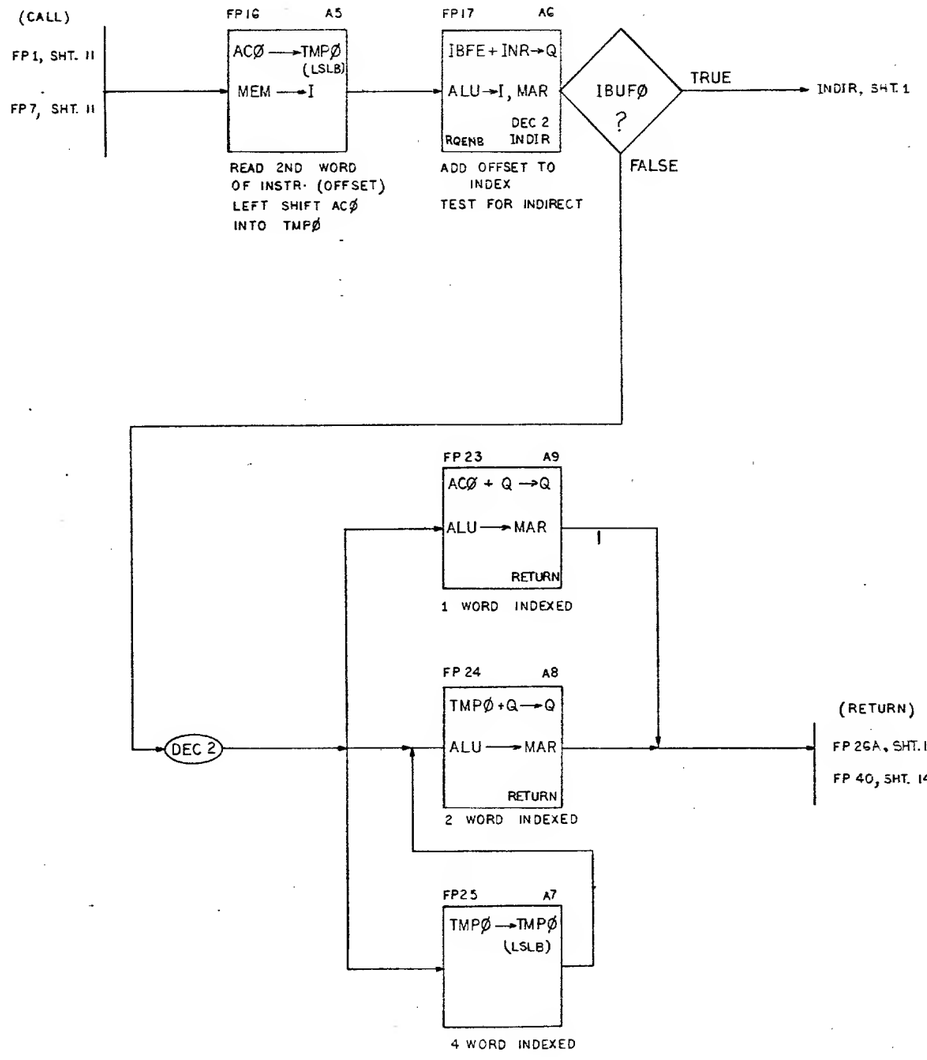
SEE SH. 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE | DWG NO. DS21E015 | UNIT WT. | SHEET 1 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730



DS21E015
E

FLOATING POINT INTERFACE
(EFA)

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1 DEG

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

DRN T. Klein 8/12
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

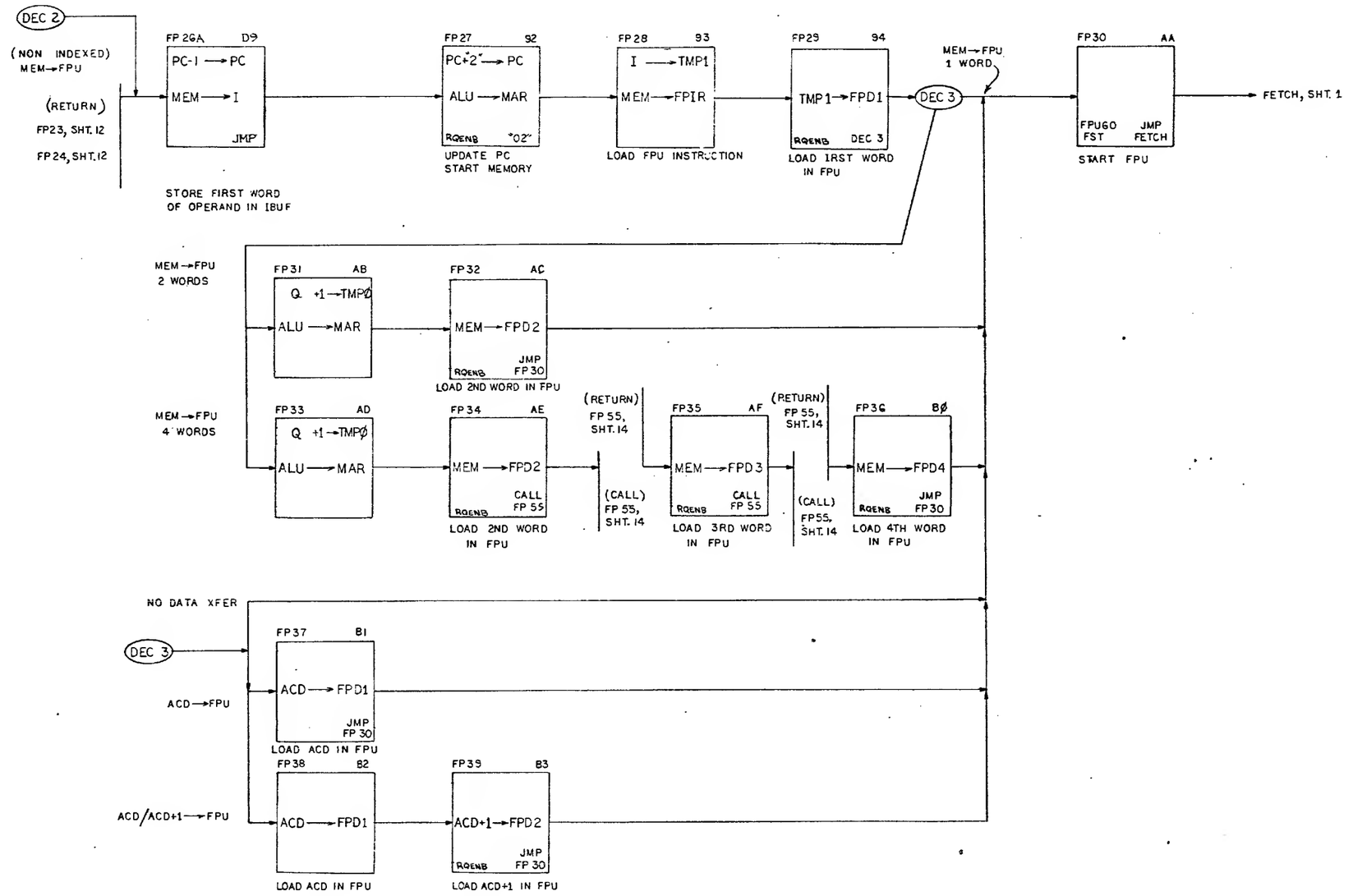
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE CVP MICROPROGRAM FLOW CHART

SCALE NONE DWG NO. DS21E015
UNIT WT.
SHEET 12 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

MARKPLACE P-3099



DSE21E015 E

FLOATING POINT INTERFACE
(MEM→FPU, ACD (S)→FPU,
NO DATA XFER)

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

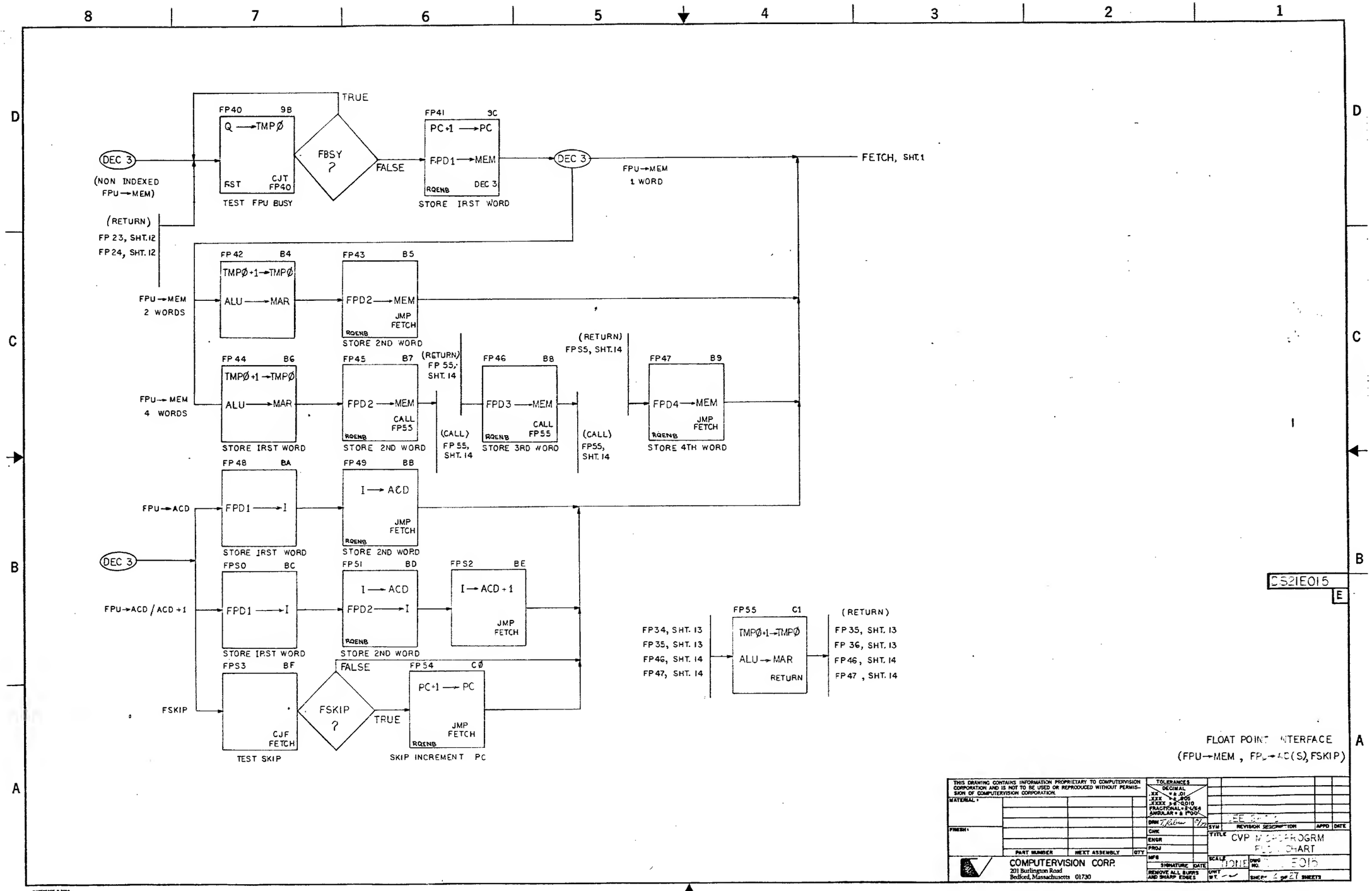
MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN T. Kelsen 9/77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1
SYM | REVISION DESCRIPTION | APPD | DATE
TITLE CVI MICRO PROGRAM FLOW CHART
SCALE NONE | DWG NO. DSE21E015
UNIT WT. ~ | SHEET 13 OF 27 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



DEC 3
(NON INDEXED FPU→MEM)
(RETURN)
FP 23, SHT. 12
FP 24, SHT. 12
FP40 9B
Q → TMPØ
FST
CJT FP40
TEST FPU BUSY
TRUE
FBSY ?
FALSE
FP41 9C
PC+1 → PC
FPD1 → MEM
RQENB
DEC 3
STORE IRST WORD
DEC 3
FPU→MEM 1 WORD
FETCH, SHT. 1
FPU→MEM 2 WORDS
FP42 B4
TMPØ+1→TMPØ
ALU → MAR
FP43 B5
FPD2 → MEM
JMP FETCH
RQENB
STORE 2ND WORD
FPU→MEM 4 WORDS
FP44 B6
TMPØ+1→TMPØ
ALU → MAR
STORE IRST WORD
FP45 B7
FPD2 → MEM
CALL FP55
RQENB
STORE 2ND WORD
(RETURN) FP 55, SHT. 14
(CALL) FP 55, SHT. 14
FP46 B8
FPD3 → MEM
CALL FP55
RQENB
STORE 3RD WORD
(RETURN) FP55, SHT. 14
(CALL) FP55, SHT. 14
FP47 B9
FPD4 → MEM
JMP FETCH
RQENB
STORE 4TH WORD
FPU→ACD
FP48 BA
FPD1 → I
STORE IRST WORD
FP49 BB
I → ACD
JMP FETCH
RQENB
STORE 2ND WORD
DEC 3
FPU→ACD / ACD+1
FPS0 BC
FPD1 → I
STORE IRST WORD
FPS1 BD
I → ACD
FPD2 → I
RQENB
STORE 2ND WORD
FPS2 BE
I → ACD+1
JMP FETCH
FSKIP
FPS3 BF
CJF FETCH
TEST SKIP
FALSE
FSKIP ?
TRUE
FP54 CØ
PC+1 → PC
JMP FETCH
RQENB
SKIP INCREMENT PC
FP34, SHT. 13
FP35, SHT. 13
FP46, SHT. 14
FP47, SHT. 14
FP55 C1
TMPØ+1→TMPØ
ALU → MAR
RETURN
(RETURN)
FP35, SHT. 13
FP36, SHT. 13
FP46, SHT. 14
FP47, SHT. 14
DS21E015
E
FLOAT POINT INTERFACE
(FPU→MEM, FPU→ACD(S), FSKIP)
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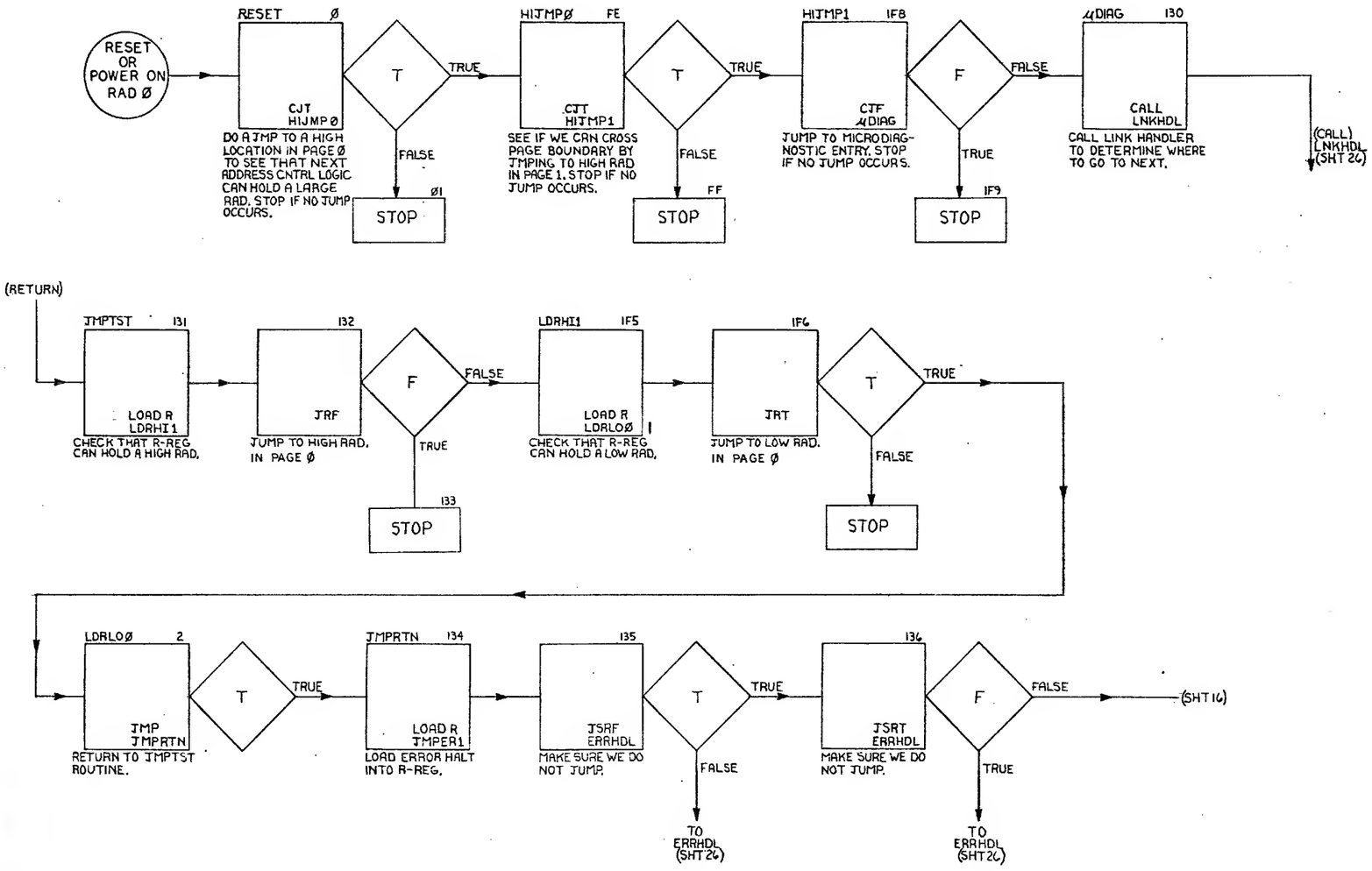
MATERIAL:
FINISH:
PART NUMBER
NEXT ASSEMBLY
QTY
TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
SYM
REVISION DESCRIPTION
APPD
DATE
TITLE
CVP MICROPROGRM FLOW CHART
SCALE NONE
DWG NO.
E015
UNIT WT.
SHEET 4 OF 27 SHEETS
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730



MICRODIAGNOSTIC ENTRY
NEXT ADDRESS CONTROL
LOGIC TEST

DS21E015
E

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TOLERANCES			
DECIMAL			
.XX ± .01			
.XXX ± .005			
.XXXX ± .0010			
FRACTIONAL ± 1/64			
ANGULAR ± 1°00'			
DRN. DAVIDSON 3-18			
CHK			
ENGR			
PROJ			
MFG			
SIGNATURE DATE			
REMOVE ALL BURRS AND SHARP EDGES			

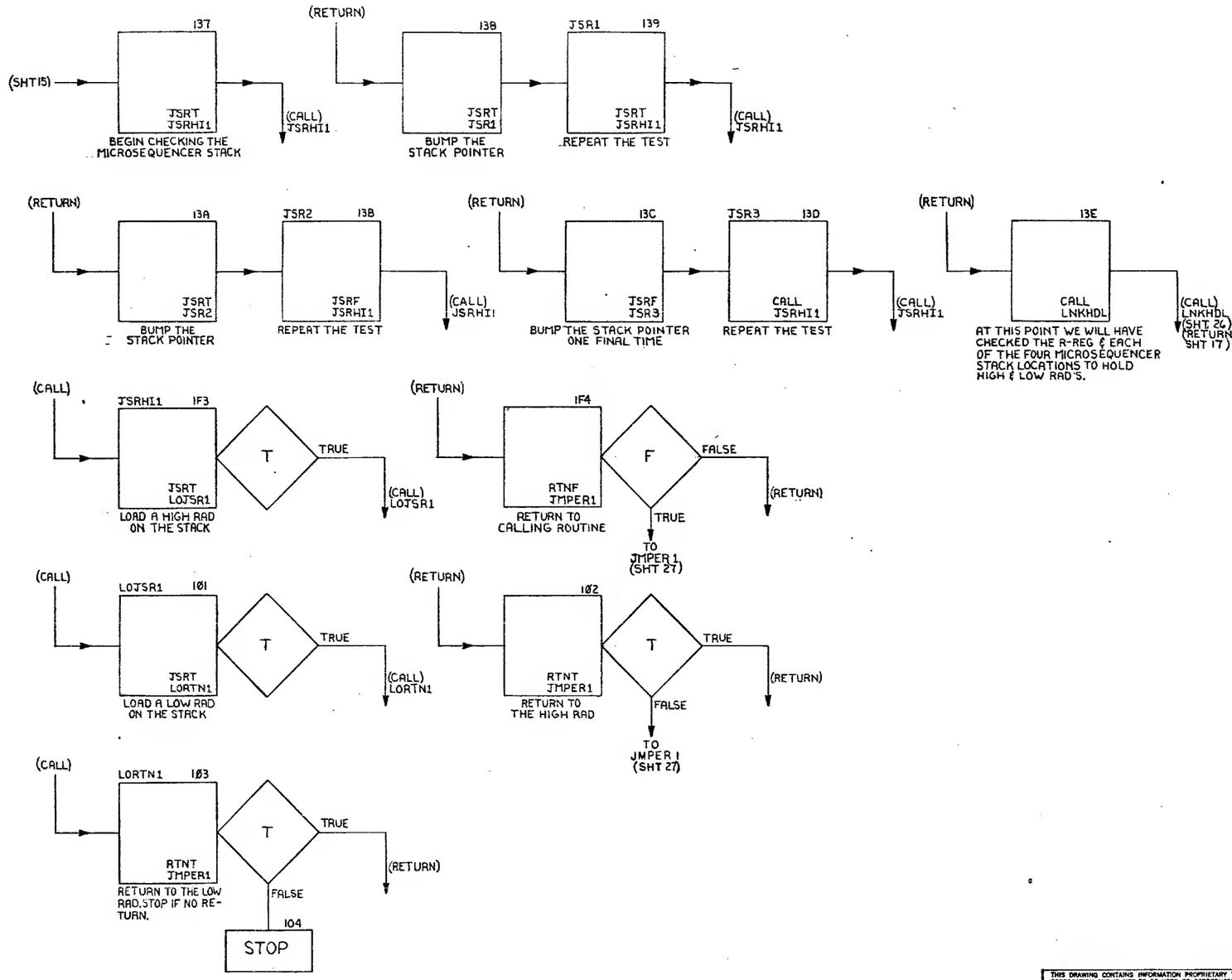
MATERIAL	PART NUMBER	NEXT ASSEMBLY	QTY
FINISH			

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHEET 1		

TITLE: FLOW CHARTS CVP MICROPROGRAM

SCALE: NONE
DWG NO. DS21E015
UNIT WT.
SHEET 15 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730



DS21E015
E

NEXT ADDRESS CONTROL
LOGIC TEST

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

BRIAN DAVIDSON 3-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: FLOW CHARTS
CVP MICROPROGRAM

SCALE: NONE
UNIT WT.:
DWG NO. DS21E015
SHEET 16 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

THIS SUBTEST CHECKS THE AZERO TEST CONDITION AND SOME BASIC ALU FUNCTIONS & DATA PATHS.

(RETURN)

RZRTST 13F
LOAD R ALUER1
LOAD R WITH ERROR HALT ADDRESS.

140
-1 TO BØ
ALU→I
JSRT ERRHDL
INIT BØ & IBUF AND CHECK AZRO ON A NON-ZERO ALU CONDITION.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

141
CLR BØ
ALU→I
JSRF ERRHDL
CLEAR BØ & IBUF AND CHECK AZRO FOR A ZERO ALU OUTPUT CONDITION. WE NOW HAVE SOME CONFIDENCE THAT AZRO CONDITION WORKS. A MORE EXTENSIVE TEST WILL BE DONE LATER, ON RZRO.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

THE FOLLOWING SERIES OF TESTS CHECKOUT THE DATA PATH FROM THE ALU TO THE IBUF THRU THE INTERNAL BUS FOR BIT PICK-UPS AND DROPS. B-PORT LOADS ARE ALSO TESTED. ALSO SOME BASIC ALU FUNCTIONS, INVERT, NEGATE (2'S COMPLIMENT), INCREMENT AND DECREMENT ARE TESTED.

DATA1 142
IBUF→Q (IBUF=Ø)
ALU→IBUF
JSRF ERRHDL
CHECK DATA PATH FROM IBUF TO ALU OUT WITH ALL ZEROES. BRANCH IF ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

143
BØ+1→BØ (BØ=1)
ALU→IBUF
JSRT ERRHDL
CHECK INCREMENT INSTRUCTIONS WITH NO CARRY. BRANCH IF ALU OUT ≠Ø; ERROR.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

NEGTS1 144
-BØ→BØ (BØ=-1)
ALU→I
JSRT ERRHDL
CHECK NEGATE INSTRUCTIONS FOR BITS STUCK AT "Ø," BRANCH IF RESULT IS ZERO; ERROR.

AZRO
TO ERRHDL (SHT 26)

145
BØ+1→BØ (BØ=Ø)
ALU→I
JSRF ERRHDL
CHECK INCREMENT INSTRUCTIONS WITH ALL CARRIES. BRANCH IF ALU OUT ≠Ø; ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

NEGTST2 146
-BØ→BØ (BØ=Ø)
ALU→I
JSRF ERRHDL
CHECK NEGATE INSTRUCTIONS FOR BITS STUCK AT "1." BRANCH IF RESULT IS ≠ZERO; ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

DATA2 147
-1→BØ
ALU→I
JSRT ERRHDL
INIT IBUF WITH ALL "1S."

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

148
IBUF+1→Q (Q=Ø)
ALU→I
JSRF ERRHDL
CHECK DATA PATH FROM IBUF TO ALU OUT WITH ALL "1'S," INCR DATA & BRANCH IF ≠Ø; ERROR.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

DECTS1 149
B-1→BØ (BØ=-2)
ALU→I
JSRT ERRHDL
CHECK DECREMENT INSTRUCTIONS WITH CARRIES. IE, 11111+11111=111110=-2 BRANCH IF =Ø; ERROR.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

14A
NOT BØ→BØ (BØ=1)
ALU→I
JSRT ERRHDL
CHECK "1'S" COMPLIMENT INSTRUCTIONS, BRANCH IF RESULT = Ø; ERROR.

AZRO
FALSE
TRUE
TO ERRHDL (SHT 26)

DECTS2 14B
BØ-1→BØ (BØ=Ø)
ALU→I
JSRF ERRHDL
CHECK DECREMENT INSTRUCTION WITH NO CARRY.

AZRO
TRUE
FALSE
TO ERRHDL (SHT 26)

14C
CALL LNKHDL
(CALL) LNKHDL (SHT 26) (RETURN SHT 18)

DS21E015
E

AZRO TEST
DATA PATH AND BASIC
ALU FUNCTION TEST

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1 POO

MATERIAL
FINISH
PART NUMBER
NEXT ASSEMBLY
QTY

DRWN D.DAVIDSON 8-78
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

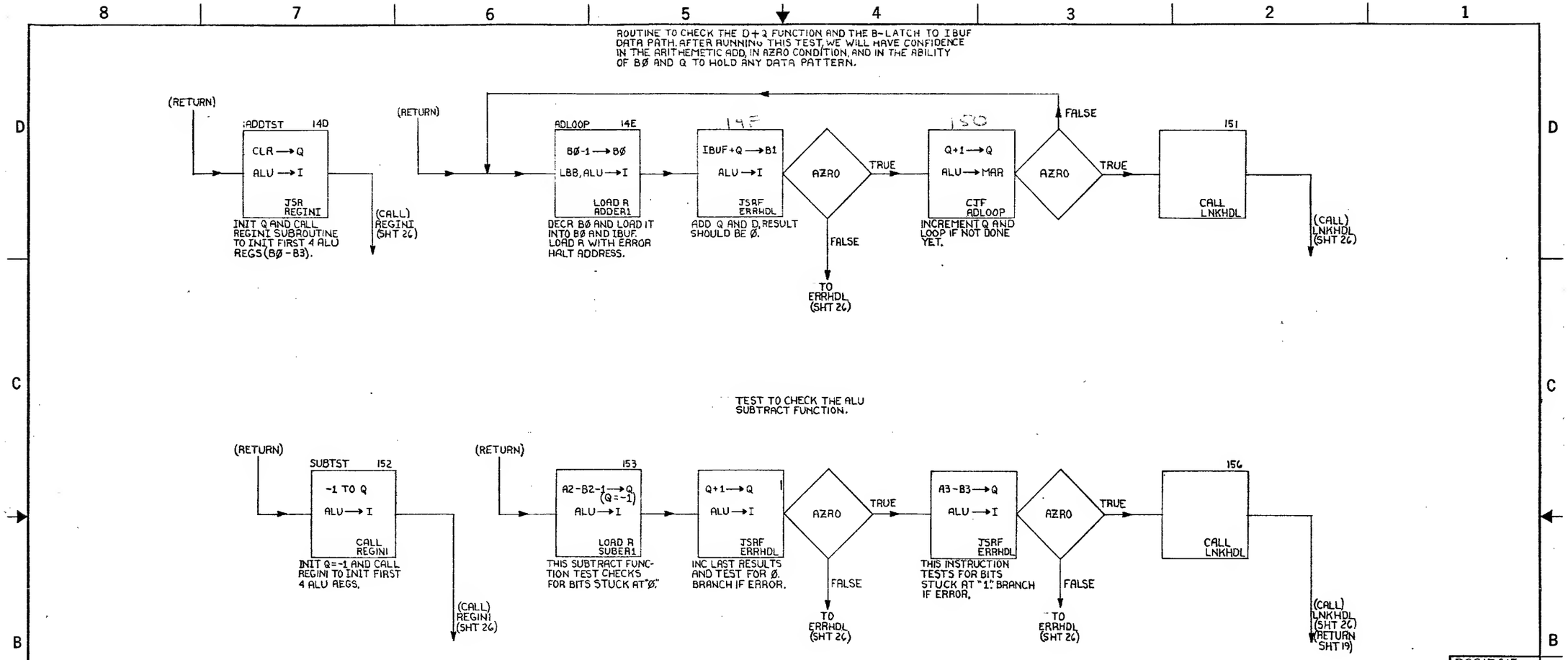
SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 17 OF 27 SHEETS

BAREFACE P-3097



ADD TEST
SUBTRACT TEST

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MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

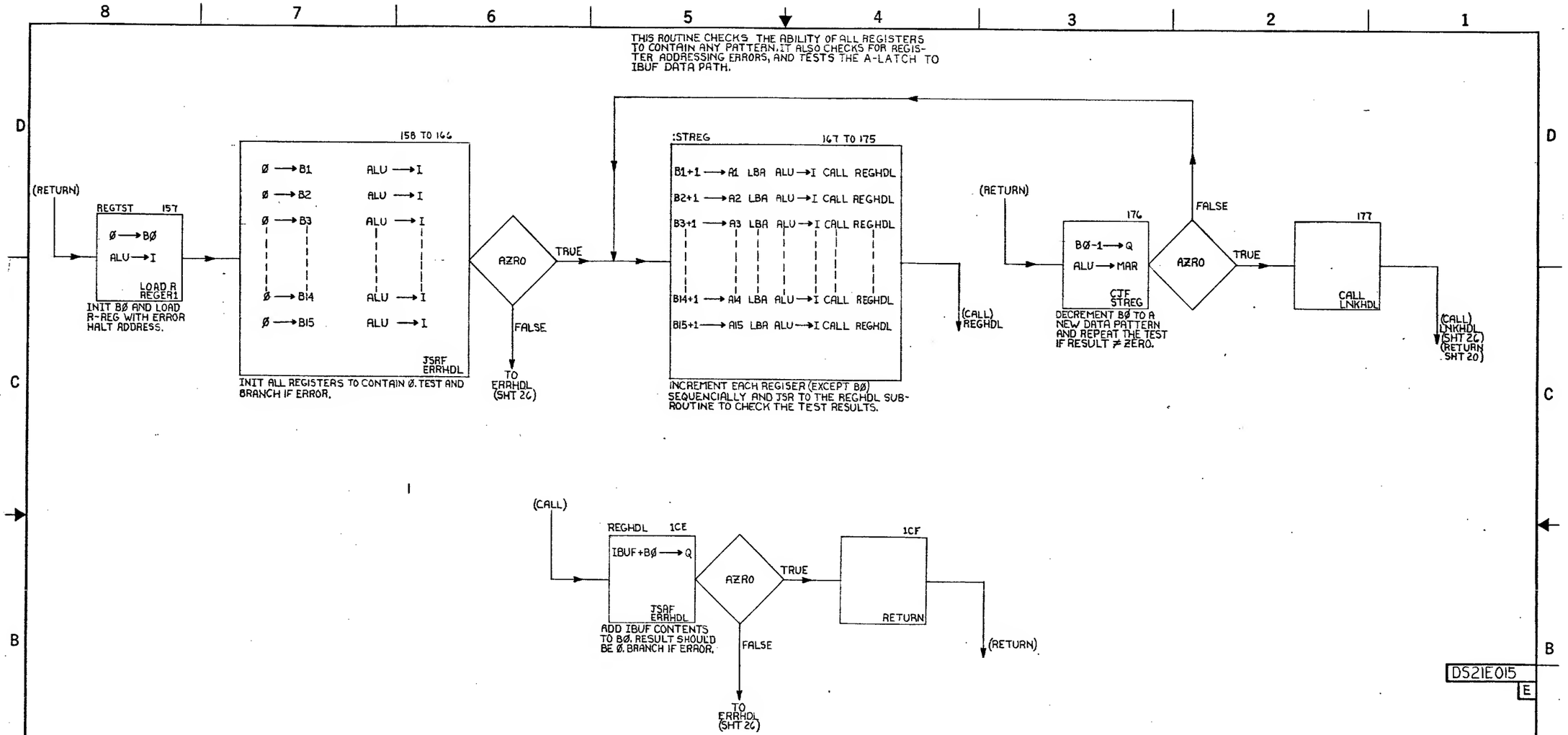
DRN D.DAVIDSON 3-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1
SYM | REVISION DESCRIPTION | APPD | DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 18 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730



ALU INTERNAL REGISTER TEST

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN D.DAVIDSON 3-78
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 19 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

THE FOLLOWING TESTS CHECK THE LOGICAL FUNCTIONS OF THE ALU.

(RETURN)

LOGIC 178

-1 TO Q

ALU → I

CALL REGINI

INIT Q AND THE FIRST 4 ALU REGISTERS.

(CALL) REGINI (SHT 26)

(RETURN)

ORTST 179

A2 V B3 → Q

ALU → I

LOAD R LOGER 1

CHECK FOR BITS STUCK AT "Ø." LOAD R WITH ERROR HALT LOCATION.

Q+1 → Q

ALU → I

JSRF ERRHDL

INCREMENT PREVIOUS RESULT TO SEE IF IT WAS -1. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 26)

AØ V BØ → Q

ALU → I

JSRF ERRHDL

CHECK FOR BITS STUCK AT "1" BY ORING Ø WITH ITSELF.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 26)

XORTST 17C

A1 ∀ B1 → Q

ALU → I

JSRF ERRHDL

XOR ALL 1'S WITH ITSELF TO CHECK FOR BITS STUCK AT "1." RESULT SHOULD = Ø. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 26)

A2 ∀ B3 → Q

ALU → I

XOR "125" & "252" PATTERN TO CHECK FOR BITS STUCK AT "Ø." RESULT SHOULD = -1.

AZRO

FALSE

TRUE

TO ERRHDL (SHT 26)

Q+1 → Q

ALU → I

JSRF ERRHDL

INCREMENT Q TO CHECK THAT LAST RESULT YIELDED THE EPECTED DATA. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 26)

RNDTST 17F

A2 ∧ B3 → Q

ALU → I

JSRF ERRHDL

AND "125" & "252" PATTERN = Ø. CHECKS FOR BITS STUCK AT "1." BRANCH IF ERROR.

RZRO

TRUE

FALSE

TO ERRHDL (SHT 26)

A1 ∧ B1 → Q

ALU → I

JSRT ERRHDL

AND ALL 1'S WITH ITSELF TO GET -1. THIS CHECKS FOR BITS STUCK AT Ø.

AZRO

FALSE

TRUE

TO ERRHDL (SHT 26)

Q+1 → Q

ALU → I

JSRF ERRHDL

INCREMENT PREVIOUS RESULT TO SEE IF IT WAS -1. BRANCH IF ERROR.

AZRO

TRUE

FALSE

TO ERRHDL (SHT 26)

182

CALL LNKHDL

(CALL) LNKHDL (SHT 26) (RETURN SHT 21)

DS21E015

E

LOGICAL ALU FUNCTION TEST

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MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES

DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN D.DAVIDSON 3-78

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE

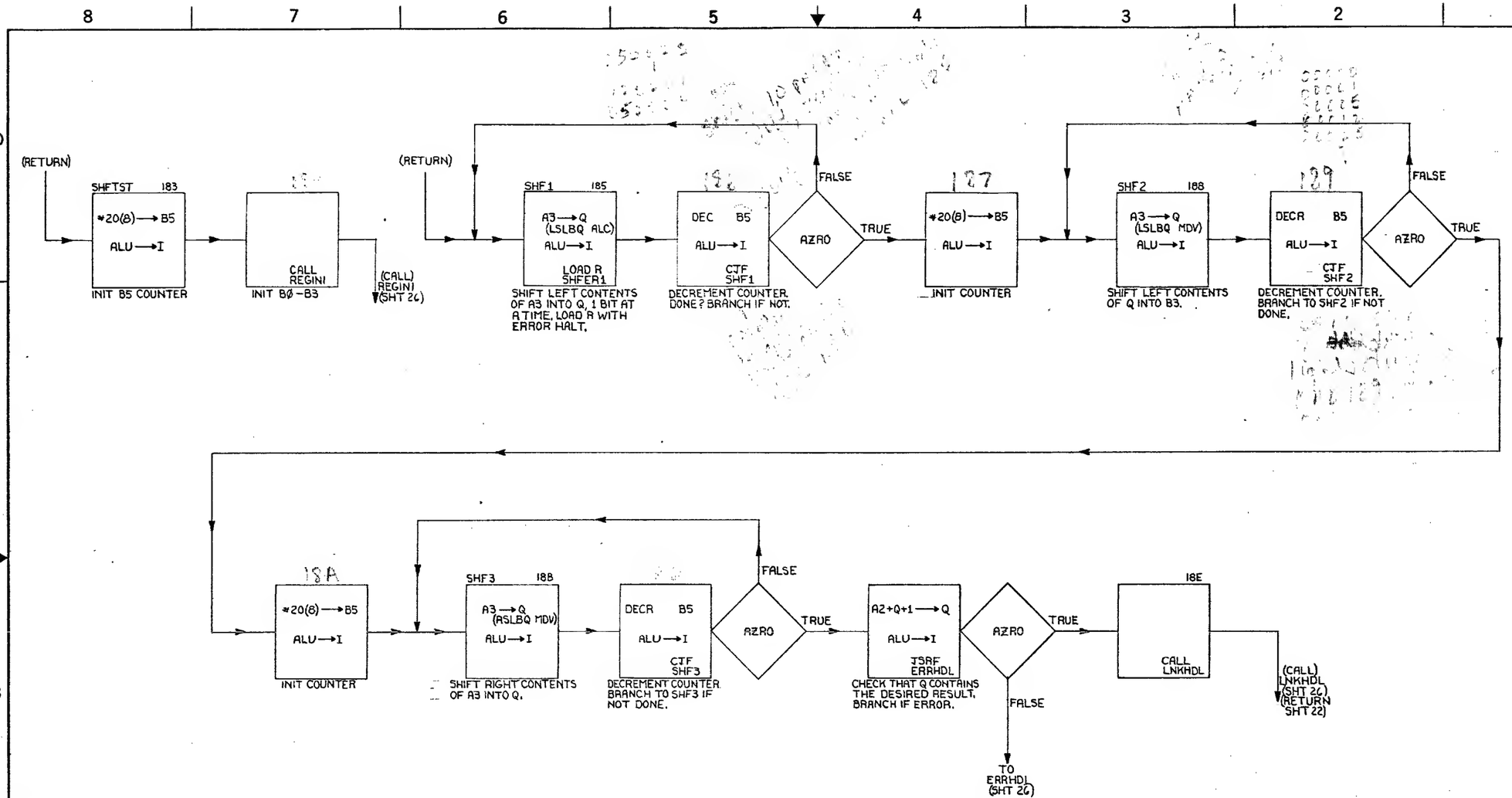
DWG NO. DS21E015

UNIT WT.

SHEET 20 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

MARKPEACE P-2079



SHIFT TEST

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL ±

FINISH ±

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRWN D.DAVIDSON 4-75
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS
CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 21 OF 27 SHEETS

COMPUTERVISION CORP.
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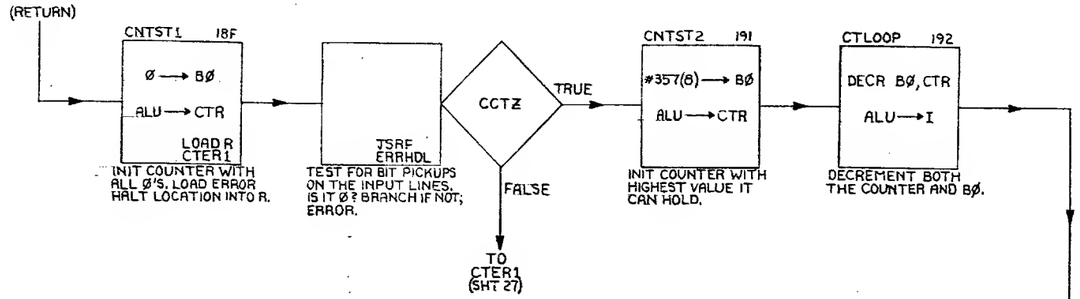
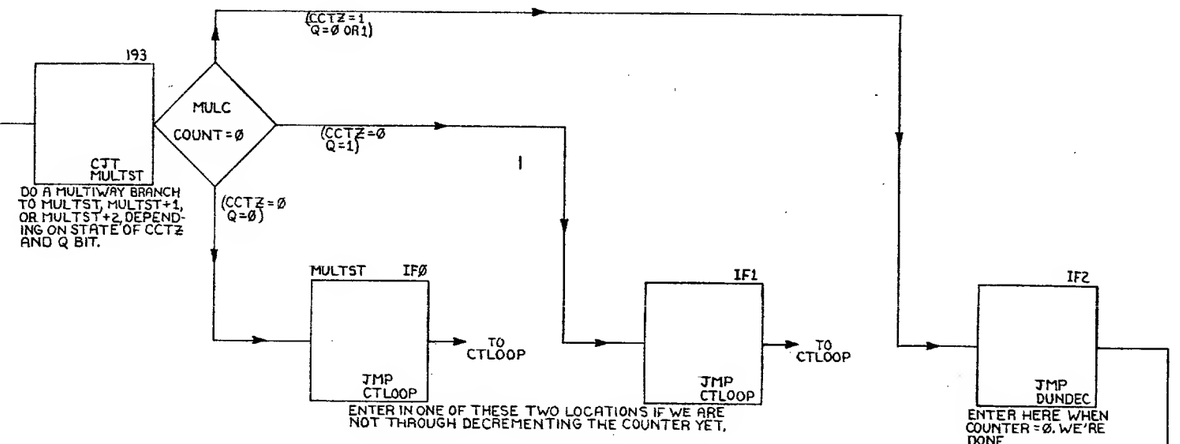
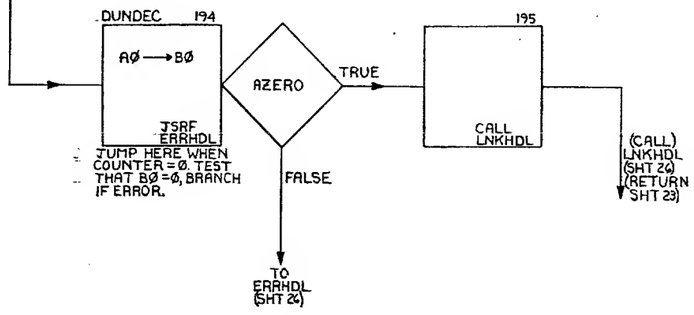
DS21E015
E

THIS SUBTEST INSURES THE INTEGRITY OF THE CPU COUNTER.







DS21E015
E

CPU COUNTER SUBTEST

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

DRWN D.DAVIDSON 4-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES
UNIT WT.

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
SHEET 22 OF 27 SHEETS

COMPUTERVISION CORP.
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MADE/FACE P-2059

TEST TO CHECK THE MEM/DATABUS "Ø" STATE, CHECK THE IR BITS Ø-7, AND CHECK THE "C" AND "CSAVE" TEST CONDITIONS.

(RETURN)

MISTST 196
MEMBUS → I
LOAD R MISER1

IBUF → Q
JSRF ERRHDL

AZERO — TRUE
FALSE → TO ERRHDL (SHT 24)

DATABUS → I

IBUF → Q
JSRF ERRHDL

AZERO — TRUE
FALSE → TO ERRHDL (SHT 24)

IRTST1 19A
#3Ø(8) → Q
ALU → I

19B
SWPI D → Q
ALU → I, IR
CALL REGINI

LOAD IR TO CHOOSE AØ AS THE SOURCE REGISTER, B3 AS THE DESTINATION REGISTER, AND TO FORCE IRØ FALSE.

→ REGINI, 5H26

RETURN ICD, SH26 →

19C
ACS → BACD (AØ → B3)
JSRT ERRHDL

TRANSFER CONTENTS OF AØ TO B3, TEST IRØ CONDITION, BRANCH IF TRUE; ERROR.

IRØ — FALSE
TRUE → TO ERRHDL (SHT 24)

-1 → BØ

INIT BØ TO PREPARE FOR NEXT TRANSFER.

#140(8) → Q
ALU → I

SWPI D → R
ALU → I, IR

LOAD IR TO CHOOSE A3 AS THE SOURCE REGISTER, BØ AS THE DESTINATION REGISTER, AND TO FORCE IR5 FALSE TEST CONDITION.

1RØ
ACS → BACD (A3 → BØ)
JSRT ERRHDL

TRANSFER CONTENTS OF A3 TO BØ. TEST IR5 CONDITION, BRANCH IF TRUE; ERROR.

IR5 — FALSE
TRUE → TO ERRHDL (SHT 24)

BØ → Q
JSRF ERRHDL

TEST BØ = Ø. BRANCH IF NOT; ERROR.

AZERO — TRUE
FALSE → TO ERRHDL (SHT 24)

#260(8) → Q
ALU → I

1A3
SWPI D → Q
ALU → I, IR

SET A-SOURC = A1, B-DESTINATION = B2, FORCE IRØ = TRUE.

1A4
ACS → BACD (A1 → B2)
JSRF ERRHDL

TRANSFER CONTENTS OF A1 TO B2. TEST IRØ TRUE, BRANCH IF ERROR.

IRØ — TRUE
FALSE → TO ERRHDL (SHT 24)

Ø → B1
ALU → I

INIT B1 TO PREPARE FOR NEXT TRANSFER.

#114(8) → Q
ALU → I
TOSTAT

SWPI D → R
ALU → I, IR
JSRT ERRHDL

SET A-SOURCE = A2, B-DESTINATION = B1, FORCE IR5 = TRUE, AND FORCE "C" FALSE TEST CONDITION, TEST "C" AND BRANCH IF ERROR.

C — FALSE
TRUE → TO ERRHDL (SHT 24)

ACS → BACD (A2 → B1)
ALU → I
JSRF ERRHDL

TRANSFER CONTENTS OF A2 TO B1. TEST IR5 TRUE, BRANCH IF ERROR.

IR5 — TRUE
FALSE → TO ERRHDL (SHT 24)

1A9
B1+1 → Q
ALU → I, IR
JSRF ERRHDL

TEST B1 FOR EXPECTED CONTENTS. BRANCH IF ERROR. THIS ALSO INITS IR FOR THE NEXT PART OF THIS TEST.

AZERO — TRUE → TO IRTST2 (SHT 24)
FALSE → TO ERRHDL (SHT 24)

DS21E015
E

MISCELLANEOUS TESTS

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MATERIAL
FINISH
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN D.DAVIDSON 4-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

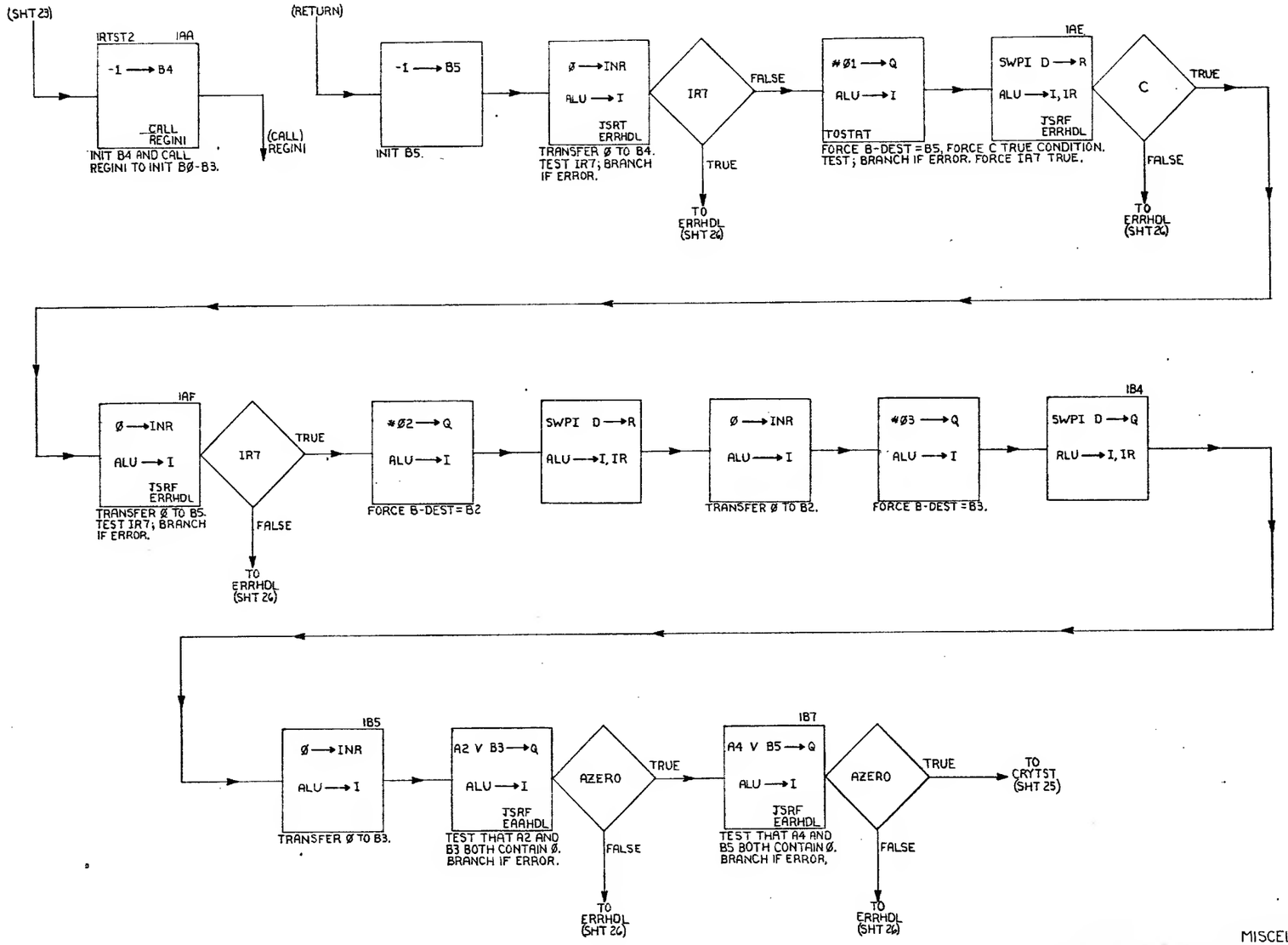
SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: FLOW CHARTS CVP MICROPROGRAM

SCALE: NONE
DWG NO. DS21E015
UNIT WT.
SHEET 23 OF 27 SHEETS

MARKPEACE P-2069



DS21E015
E

MISCELLANEOUS TESTS

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TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

MATERIAL
FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

DRN D.DAVIDSON 5-78
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE: FLOW CHARTS CVP MICROPROGRAM

SCALE NONE | DWG NO. DS21E015 | REV

UNIT WT. | SHEET 24 OF 27 SHEETS

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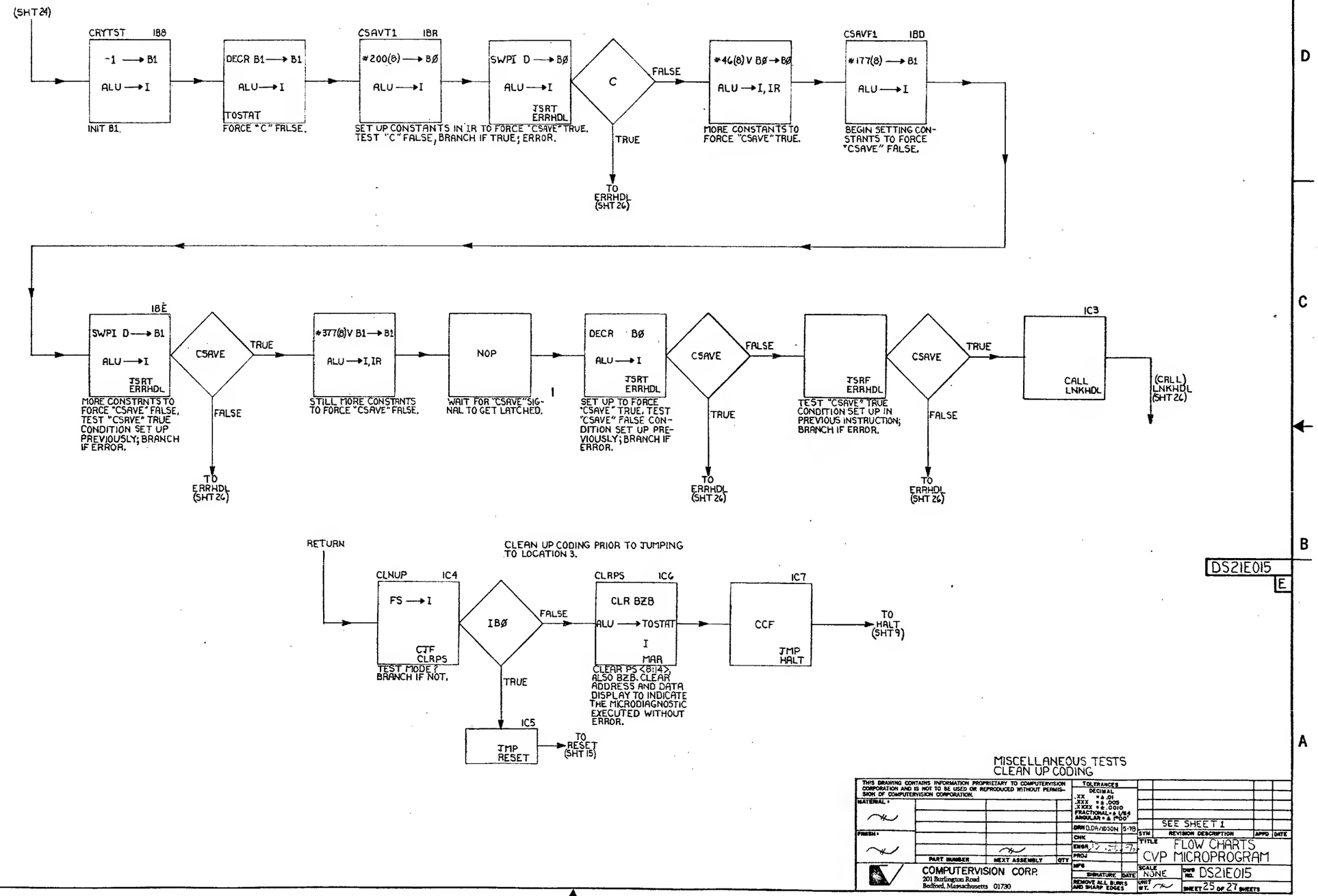
Bedford, Massachusetts 01730


(SHT 24)
CRYTST IB8
-1 → B1
ALU → I
INIT B1.
DECR B1 → B1
ALU → I
TOSTAT
FORCE "C" FALSE.
CSAVT1 IBR
#200(8) → BØ
ALU → I
SET UP CONSTANTS IN IR TO FORCE "CSAVE" TRUE. TEST "C" FALSE, BRANCH IF TRUE; ERROR.
SWPI D → BØ
ALU → I
JSRT ERRHDL
C
FALSE
TRUE
TO ERRHDL (SHT 26)
#46(8) V BØ → BØ
ALU → I, IR
MORE CONSTANTS TO FORCE "CSAVE" TRUE.
CSAVF1 IBD
#177(8) → B1
ALU → I
BEGIN SETTING CONSTANTS TO FORCE "CSAVE" FALSE.
IBE
SWPI D → B1
ALU → I
JSRT ERRHDL
MORE CONSTANTS TO FORCE "CSAVE" FALSE, TEST "CSAVE" TRUE CONDITION SET UP PREVIOUSLY; BRANCH IF ERROR.
CSAVE
TRUE
FALSE
TO ERRHDL (SHT 24)
#377(8) V B1 → B1
ALU → I, IR
STILL MORE CONSTANTS TO FORCE "CSAVE" FALSE.
NOP
WAIT FOR "CSAVE" SIGNAL TO GET LATCHED.
DECR BØ
ALU → I
JSRT ERRHDL
SET UP TO FORCE "CSAVE" TRUE. TEST "CSAVE" FALSE CONDITION SET UP PREVIOUSLY; BRANCH IF ERROR.
CSAVE
FALSE
TRUE
TO ERRHDL (SHT 24)
JSRF ERRHDL
TEST "CSAVE" TRUE CONDITION SET UP IN PREVIOUS INSTRUCTION; BRANCH IF ERROR.
CSAVE
TRUE
FALSE
TO ERRHDL (SHT 24)
IC3
CALL LNKHDL
(CALL) LNKHDL (SHT 26)
RETURN
CLEAN UP CODING PRIOR TO JUMPING TO LOCATION 3.
CLNUP IC4
FS → I
CTF CLRPS
TEST MODE ? BRANCH IF NOT.
IBØ
FALSE
TRUE
CLRPS IC6
CLR BZB
ALU → TOSTAT
I
MAR
CLEAR PS <8:14> ALSO BZB. CLEAR ADDRESS AND DATA DISPLAY TO INDICATE THE MICRODIAGNOSTIC EXECUTED WITHOUT ERROR.
IC7
CCF
JMP HALT
TO HALT (SHT 9)
IC5
JMP RESET
TO RESET (SHT 15)
MISCELLANEOUS TESTS
CLEAN UP CODING
DS21E015
E
SEE SHEET 1
FLOW CHARTS
CVP MICROPROGRAM
DS21E015
SHEET 25 OF 27 SHEETS
COMPUTERVISION CORP.
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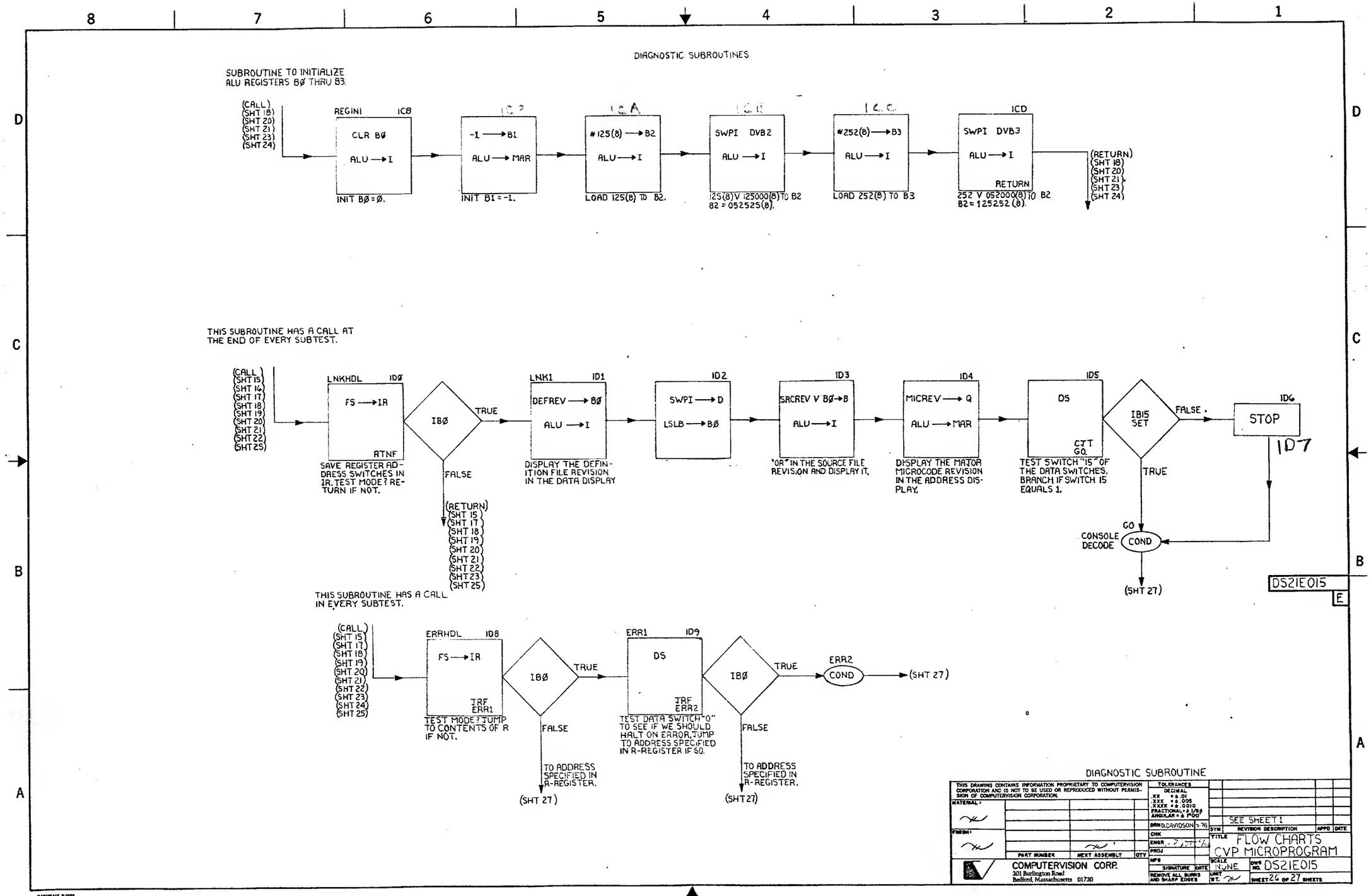
Bedford, Massachusetts 01730


DIAGNOSTIC SUBROUTINES
SUBROUTINE TO INITIALIZE ALU REGISTERS BØ THRU B3.
(CALL) (SHT 18) (SHT 20) (SHT 21) (SHT 23) (SHT 24)
REGINI IC8
CLR BØ
ALU → I
INIT BØ = Ø.
-1 → B1
ALU → MAR
INIT B1 = -1.
#125(8) → B2
ALU → I
LOAD 125(8) TO B2.
SWPI DVB2
ALU → I
125(8) V 125000(8) TO B2
B2 = 052525(8).
#252(8) → B3
ALU → I
LOAD 252(8) TO B3
ICD
SWPI DVB3
ALU → I
RETURN
252 V 052000(8) TO B2
B2 = 125252 (8).
(RETURN) (SHT 18) (SHT 20) (SHT 21) (SHT 23) (SHT 24)
THIS SUBROUTINE HAS A CALL AT THE END OF EVERY SUBTEST.
(CALL) (SHT 15) (SHT 16) (SHT 17) (SHT 18) (SHT 19) (SHT 20) (SHT 21) (SHT 22) (SHT 25)
LNKHDL ID0
FS → IR
RTNF
SAVE REGISTER ADDRESS SWITCHES IN IR. TEST MODE? RETURN IF NOT.
IBØ
TRUE
FALSE
(RETURN) (SHT 15) (SHT 17) (SHT 18) (SHT 19) (SHT 20) (SHT 21) (SHT 22) (SHT 23) (SHT 25)
LNK1 ID1
DEFREV → BØ
ALU → I
DISPLAY THE DEFINITION FILE REVISION IN THE DATA DISPLAY
ID2
SWPI → D
LSLB → BØ
ID3
SRCREV V BØ → B
ALU → I
"OR" IN THE SOURCE FILE REVISION AND DISPLAY IT.
ID4
MICREV → Q
ALU → MAR
DISPLAY THE MAJOR MICROCODE REVISION IN THE ADDRESS DISPLAY.
ID5
DS
CTT GO
TEST SWITCH "15" OF THE DATA SWITCHES. BRANCH IF SWITCH 15 EQUALS 1.
IB15 SET
FALSE
TRUE
ID6
STOP
ID7
GO
CONSOLE DECODE
COND
(SHT 27)
DS21E015
E
THIS SUBROUTINE HAS A CALL IN EVERY SUBTEST.
(CALL) (SHT 15) (SHT 17) (SHT 18) (SHT 19) (SHT 20) (SHT 21) (SHT 22) (SHT 23) (SHT 24) (SHT 25)
ERRHDL ID8
FS → IR
JRF ERR1
TEST MODE? JUMP TO CONTENTS OF R IF NOT.
IBØ
TRUE
FALSE
TO ADDRESS SPECIFIED IN R-REGISTER.
(SHT 27)
ERR1 ID9
DS
JRF ERR2
TEST DATA SWITCH "0" TO SEE IF WE SHOULD HALT ON ERROR, JUMP TO ADDRESS SPECIFIED IN R-REGISTER IF SO.
IBØ
TRUE
FALSE
TO ADDRESS SPECIFIED IN R-REGISTER.
(SHT 27)
ERR2
COND
(SHT 27)
DIAGNOSTIC SUBROUTINE
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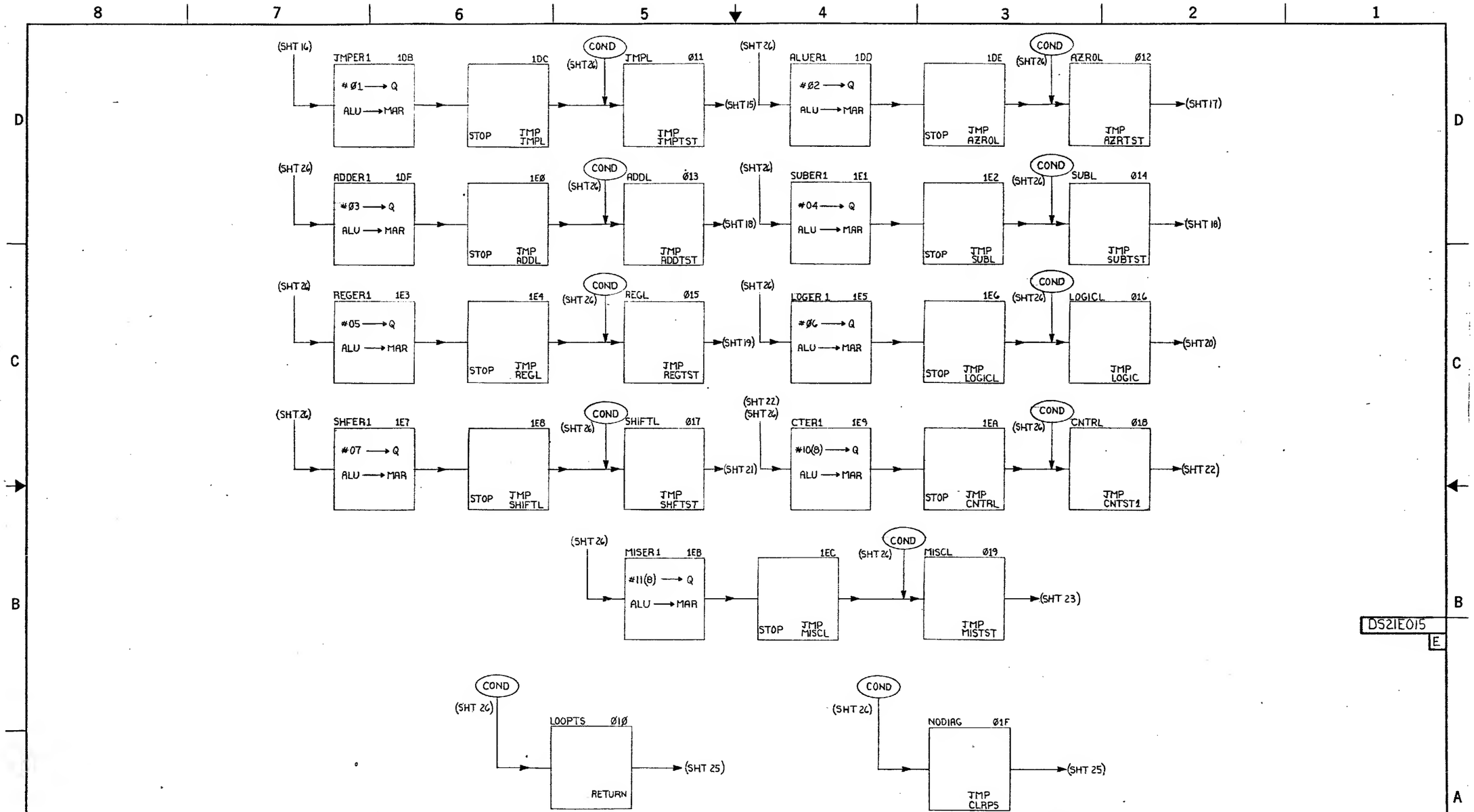
MATERIAL:
FINISH:
PART NUMBER
NEXT ASSEMBLY
QTY
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730
TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'
DRN D.DAVIDSON 5-78
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SHEET 1
SYM
REVISION DESCRIPTION
APPD
DATE
TITLE FLOW CHARTS CVP MICROPROGRAM
SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 26 OF 27 SHEETS



ERROR HALTS AND COND LINKS

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:

FINISH:

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN D.DAVIDSON 5-78
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE FLOW CHARTS CVP MICROPROGRAM

SCALE NONE
DWG NO. DS21E015
UNIT WT.
SHEET 27 OF 27 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

128/32K A/B-Port Memory Unit
DS21E252

	Sheet No.
Address Selection	1
Jumper Configuration	1
Memory Prioritizing	2
Refresh and Timing Logic	2
Data In Multiplexer	3
Data Out Latch	3
Parity Logic	3
Bus Control Logic	4
Bus Logic	5
Memory Address Logic	5
A-Port/B-Port Select Logic	6
Address Multiplexer Logic	6
Refresh Counter Logic	6
Row Address Strobe Clock	6
I/O Logic	7
Memory Row A	8
Memory Row B	9
Memory Row C	10
Memory Row D	11
Memory Row E	12
Memory Row F	13
Memory Row G	14
Memory Row H	15
B-Port Connectors	16

DA21E250-X CONFIGURATION TABLE

	SINGLE PORT	DUAL PORT, DISTRIBUTED MODE	DUAL PORT, GPU MODE	SINGLE PORT 32K
POPULATED WITH 4K RAMS (MK 4027-3)	USE CONFIGURATION BLOCKS A,A1,B	USE CONFIGURATION BLOCKS A,A1,C,D,E	USE CONFIGURATION BLOCKS A,C,D,E	
POPULATED WITH 16K RAMS (MK 4116-3)	DA21E250-02 USE CONFIGURATION BLOCKS B,F	DA21E250-01 USE CONFIGURATION BLOCKS D,E,F,G	DA21E250-01 USE CONFIGURATION BLOCKS E,F,H	DA21E250-03 USE CONFIGURATION BLOCKS A1,I

CONFIGURATION BLOCK A) 32K HARDWARE CONFIGURATION (USING 4K RAMS)

1) REMOVE R22
2) ADJUST POT R31 SUCH THAT TP HAS A 29 µS REP RATE
3) INSERT JUMPERS: JP9-2 , JP11-2 , JP13-2
4) POPULATE MEMORY ARRAY WITH MK4027-3 MEMORY CHIPS

CONFIGURATION BLOCK A1) APORT 32K ADDRESSING CHART

*APORT FIELD	AMC0	AMC1	AMC2	AMC3	**CLOSED CONTACTS ON SWITCH PACK 1V
0	H	H	H	H	8
1	H	H	H	L	7,8
2	H	H	L	H	8,B
3	H	H	L	L	8,7,8
4	H	L	H	H	5,8
5	H	L	H	L	5,7,8
6	H	L	L	H	5,8,8
7	H	L	L	L	5,8,7,8
8	L	H	H	H	4,8
9	L	H	H	L	4,7,8
10	L	H	L	H	4,8,8
11	L	H	L	L	4,B,7,8
12	L	L	H	H	4,5,8
13	L	L	H	L	4,5,7,8
14	L	L	L	H	4,5,B,B
15	L	L	L	L	4,5,B,7,8

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 1V OPEN

CONFIGURATION BLOCK B) SINGLEPORT CONFIGURATION

1) DEPOPULATE PC BOARD AS PER BM21E250-02
2) ADD JUMPERS JP3 , JP5 , JP7

CONFIGURATION BLOCK C) BPORT 32K MEMORY ROW SELECT

1) INSERT JUMPERS: JP10-2 , JP12-2 , JP14-2

CONFIGURATION BLOCK D) BPORT 32K ADDRESSING AND I/O DEVICE CODE CHART

*BPORT FIELD OR I/O DEVICE CODE	BMC0 OR BDS0	BMC1 OR BDS1	BMC2 OR BDS2	BMC3 OR BDS3	**CLOSED CONTACTS ON SWITCH PACK 12S
0	H	H	H	H	8
1	H	H	H	L	4,8
2	H	H	L	H	3,8
3	H	H	L	L	3,4,8
4	H	L	H	H	2,8
5	H	L	H	L	2,4,8
6	H	L	L	H	2,3,8
7	H	L	L	L	2,3,4,8
8	L	H	H	H	1,8
9	L	H	H	L	1,4,8
10	L	H	L	H	1,3,8
11	L	H	L	L	1,3,4,8
12	L	L	H	H	1,2,8
13	L	L	H	L	1,2,4,8
14	L	L	L	H	1,2,3,8
15	L	L	L	L	1,2,3,4,8

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN

CONFIGURATION BLOCK E) LAST BOARD IN DAISY CHAIN

THE LAST DUAL PORT MEMORY BOARD IN A DAISY CHAIN MUST TERMINATE BPORT BUS SIGNALS. THE LAST DUAL PORT MEMORY IN A DAISY CHAIN ONLY MUST HAVE THE FOLLOWING RESISTORS: RP6,RP7,RP8, RP12 , RES PACK 12F

CONFIGURATION BLOCK F) 128K HARDWARE CONFIGURATION/APORT 128K ADDRESSING M

1) R20 AND R22 INSERTED
2) INSERT JIMPER JP4
3) ADJUST POT R31 SUCH THAT TP HAS A 14.5 µS REP RATE
4) INSERT JUMPERS JP9 , JP11 , JP13
5) POPULATE MEMORY ARRAY WITH MK411B-3 MEMORY CHIPS
6) APORT 128K ADDRESSING CHART

*APORT FIELD NO.	$\overline{AMC0}$	$\overline{AMC1}$	$\overline{AMC2}$	$\overline{AMC3}$	$\overline{AMC3}$	**CLOSED CONTACTS ON SWITCH PACK 1V
0,1,2,3	H	H	H	H	H	
4,5,6,7	H	H	H	H	L	5
8,9,10,11	H	H	H	L	H	4
12,13,14,15	H	H	H	L	L	4,5
16,17,1B,19	H	H	L	H	H	3
20,21,22,23	H	H	L	H	L	3,5
24,25,26,27	H	H	L	L	H	3,4
28,29,30,31	H	H	L	L	L	3,4,5
32,33,34,35	H	L	H	H	H	2
36,37,38,39	H	L	H	H	L	2,5
40,41,42,43	H	L	H	L	H	2,4
44,45,4B,47	H	L	H	L	L	2,4,5
48,49,50,51	H	L	L	H	H	2,3
52,53,54,55	H	L	L	H	L	2,3,5
58,57,58,59	H	L	L	L	H	2,3,4
60,61,62,63	H	L	L	L	L	2,3,4,5
64,65,66,67	L	H	H	H	H	1
68,69,70,71	L	H	H	H	L	1,5
72,73,74,75	L	H	H	L	H	1,4
7B,77,7B,79	L	H	H	L	L	1,4,5
80,81,82,83	L	H	L	H	H	1,3
84,85,8B,B7	L	H	L	H	L	1,3,5
88,89,90,91	L	H	L	L	H	1,3,4
92,93,94,95	L	H	L	L	L	1,3,4,5
98,97,98,99	L	L	H	H	H	1,2
100,101,102,103	L	L	H	H	L	1,2,5
104,105,108,107	L	L	H	L	H	1,2,4
108,109,110,111	L	L	H	L	L	1,2,4,5
112,113,114,115	L	L	L	H	H	1,2,3
118,117,118,119	L	L	L	H	L	1,2,3,5
120,121,122,123	L	L	L	L	H	1,2,3,4
124,125,12B,127	L	L	L	L	L	1,2,3,4,5

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY (TO EXPAND BEYOND 15 FIELDS , IC 2X AND 2V , SHT.7 , MUST BE ADDED)
** ALL OTHER SWITCH CONTACTS ON SWITCH 1V ARE OPEN

CONFIGURATION BLOCK G) 12BK APORT/32K BPORT COMMON MEMORY

WITH JUMPERS JP10, JP12, JP14, INSERTED

$\overline{BMC2}$	$\overline{BMC3}$	COMMON SEGMENT OF APORT 12BK MEMORY
H	H	1ST 32K
H	L	2ND 32K
L	H	3RD 32K
L	L	4TH 32K

2) TO FORCE COMMON APORT/BPORT MEMORY INDEPENDENT OF BMC2 AND BMC3

$\overline{BMC2}$	$\overline{BMC3}$	COMMON SEGMENT OF APORT 12BK MEMORY	JUMPERS INSERTED
X	X	1ST 32K	JP10, JP15, JP1B
X	X	2ND 32K	JP10, JP1B
X	X	3RD 32K	JP10, JP15
X	X	4TH 32K	JP10

WHERE X = DONT CARE

CONFIGURATION BLOCK H) BPORT 128K ADDRESSING CONFIGURATION

1) INSERT JUMPERS JP10, JP12, JP14
2) BPORT 128K ADDRESSING CHART

BPORT FIELD NO.	BMAD0	BMAD1	BMAD2	BMC0	BMC1	**CLOSED CONTACTS ON SWITCH PACKS	
						9C	12S
0,1,2,3	H	H	H	H	H		8
4,5,B,7	H	H	H	H	L		2,8
8,9,10,11	H	H	H	L	H		1,8
12,13,14,15	H	H	H	L	L		1,2,8
1B,17,1B,19	H	H	L	H	H	7	8
20,21,22,23	H	H	L	H	L	7	2,8
24,25,28,27	H	H	L	L	H	7	1,8
28,29,30,31	H	H	L	L	L	7	1,2,8
32,33,34,35	H	L	H	H	H	8	8
38,37,38,39	H	L	H	H	L	8	2,8
40,41,42,43	H	L	H	L	H	8	1,8
44,45,4B,47	H	L	H	L	L	8	1,2,8
4B,49,50,51	H	L	L	H	H	8,7	8
52,53,54,55	H	L	L	H	L	8,7	2,8
58,57,58,59	H	L	L	L	H	8,7	1,8
80,81,82,83	H	L	L	L	L	8,7	1,2,8
84,85,8B,87	L	H	H	H	H	5	8
88,89,70,71	L	H	H	H	L	5	2,8
72,73,74,75	L	H	H	L	H	5	1,8
78,77,78,79	L	H	H	L	L	5	1,2,8
80,81,82,83	L	H	L	H	H	5,7	8
84,85,88,87	L	H	L	H	L	5,7	2,8
88,89,90,91	L	H	L	L	H	5,7	1,8
92,93,94,95	L	H	L	L	L	5,7	1,2,8
98,97,98,99	L	L	H	H	H	5,8	8
100,101,102,103	L	L	H	H	L	5,8	2,8
104,105,108,107	L	L	H	L	H	5,8	1,8
108,109,110,111	L	L	H	L	L	5,8	1,2,8
112,113,114,115	L	L	L	H	H	5,B,7	8
11B,117,118,119	L	L	L	H	L	5,8,7	2,8
120,121,122,123	L	L	L	L	H	5,8,7	1,8
124,125,12B,127	L	L	L	L	L	5,8,7	1,2,8

EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN
(9C-2 MAY BE CLOSED TO DISABLE APORT)

CONFIGURATION BLOCK I) 32K SINGLE PORT CONFIGURATION (USING 16K RAMS)

1) DEPOPULATE BOARDS AS PER ASSEMBLY DA21E250-03

MISCELLANEOUS JUMPERS

1) FOR LDMAR STARTING APORT MEMORY CYCLE INSERT JP-2
2) FOR MEMREAD STARTING APORT MEMORY CYCLE INSERT JP-1
3) FOR GPU MODE REQUIRING DISABLED APORT , CLOSE SWITCH 9C-2
4) APORT MUC/NON MUC OPERATION

JUMPER PLUG 4D	
MUC OPERATION	1-18 2-16 3-14 4-13
NON MUC OPERATION	5-12 6-11 7-10 8-9

5) APORT I/O DEVICE CODE

1) STANDARD 24_8. INSERT JP8 FOR 25_8

DS21E252
E

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
XX ±.01
XXX ±.005
XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100

MATERIAL: N/A
FINISH: N/A
PART NUMBER: DA21E250 | NEXT ASSEMBLY: 1 | QTY

DRN: B HOBBS 7/7/81
CHK: [illegible] 7/7/81
ENGR: M Santos 7/7/81
PROJ: J McAnney 7/7/81
MFG
SIGNATURE | DATE

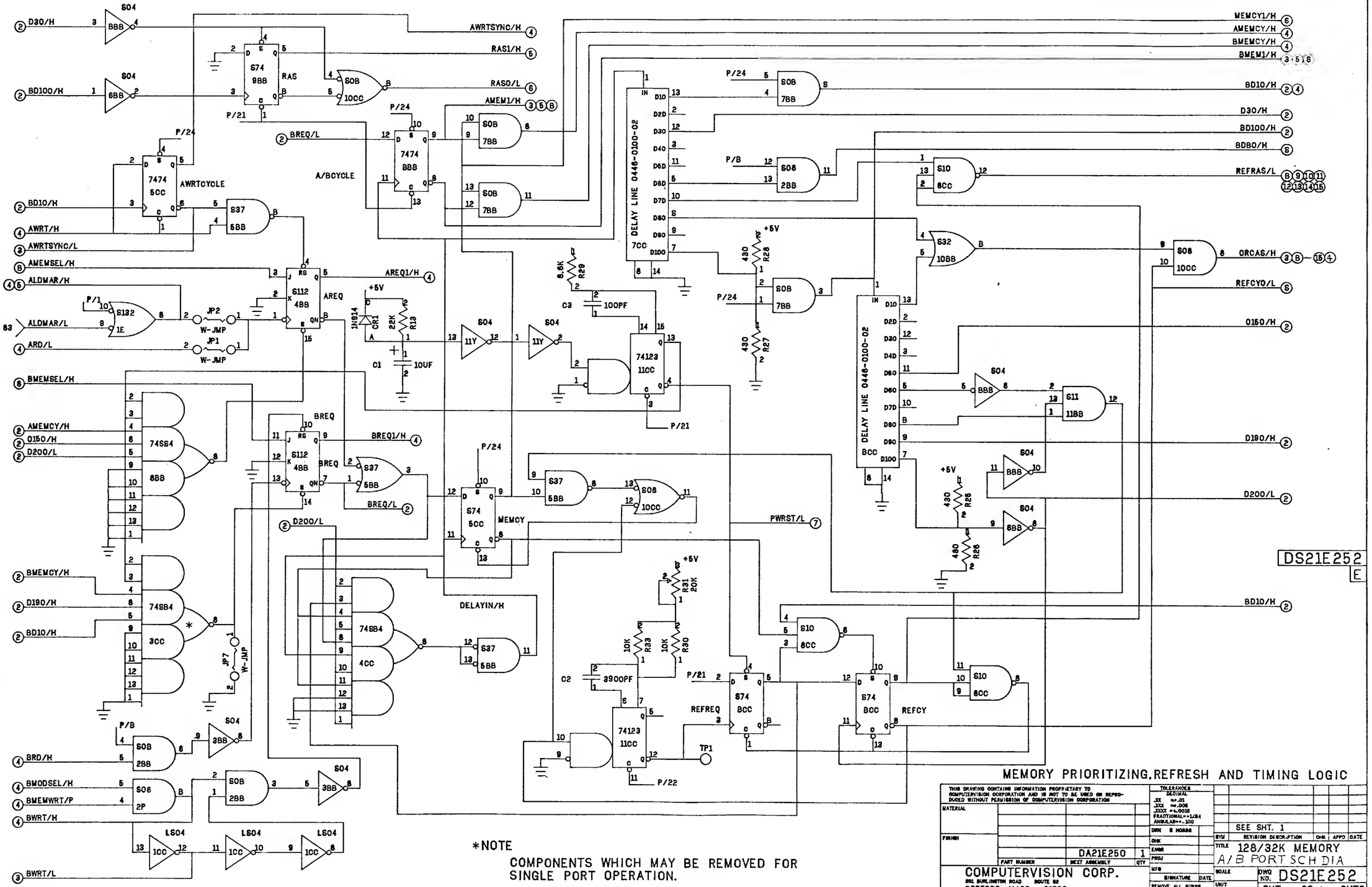
REMOVE ALL BURRS AND SHARP EDGES

E	ECO 3423	[illegible]	[illegible]	[illegible]
D	ECO 3338	[illegible]	[illegible]	[illegible]
SYM	REVISION DESCRIPTION	DRN	APPD	DATE

TITLE: 128/32K MEMORY A/BPORT SCHEMATIC DIAGRAM

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 1 OF 16 SHTS

COMPUTERVISION CORP.
300 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730



*NOTE

COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

DS21E252
E

MEMORY PRIORITIZING, REFRESH AND TIMING LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0050 FRACTIONAL ±1/64 ANGULAR ±.100

MATERIAL

FINISH

DRN S HOBBS

CHK

ENGR

PROJ

MFR

DA21E250 1

PART NUMBER NEXT ASSEMBLY QTY

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

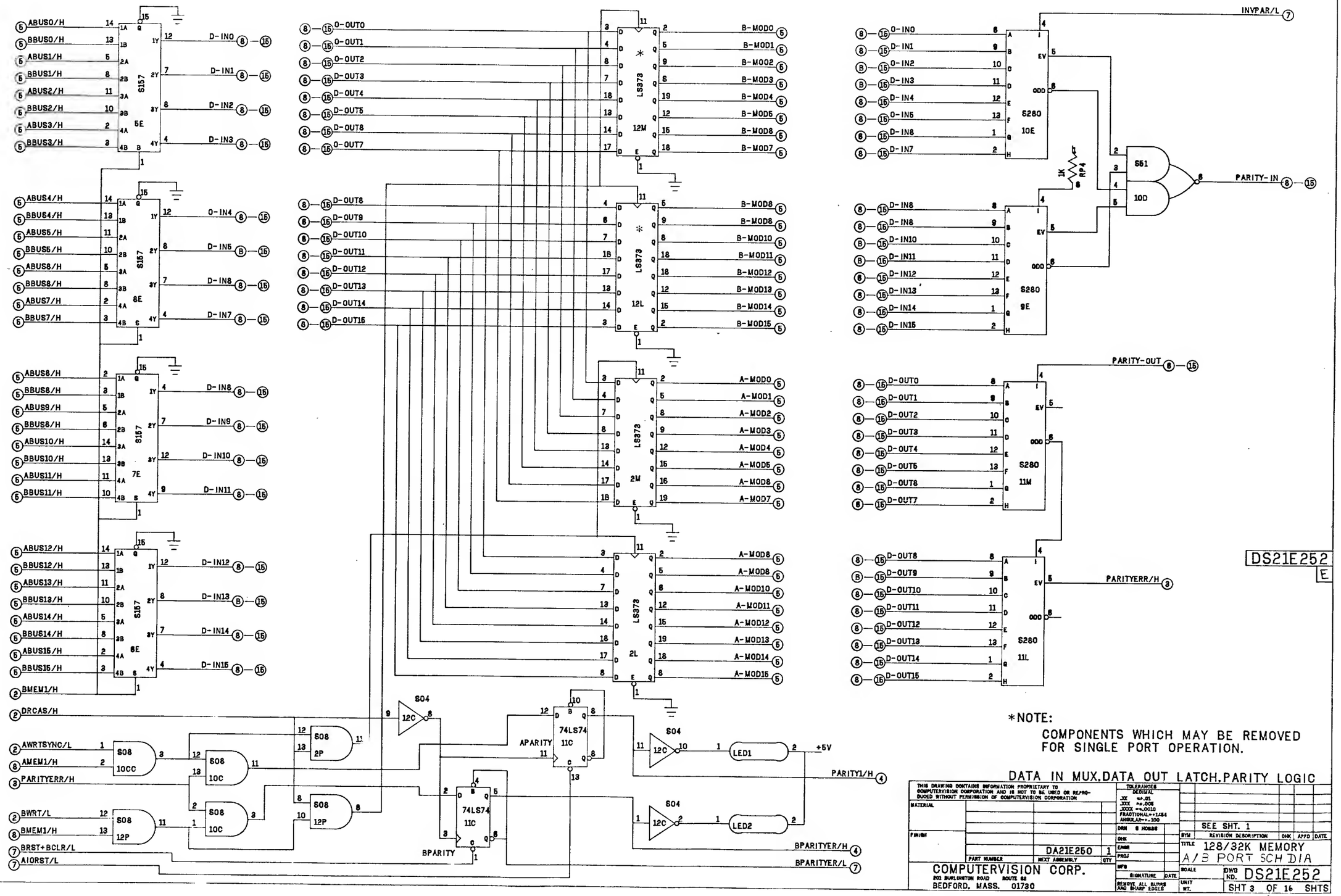
TITLE 128/32K MEMORY A/B PORT SCH DIA

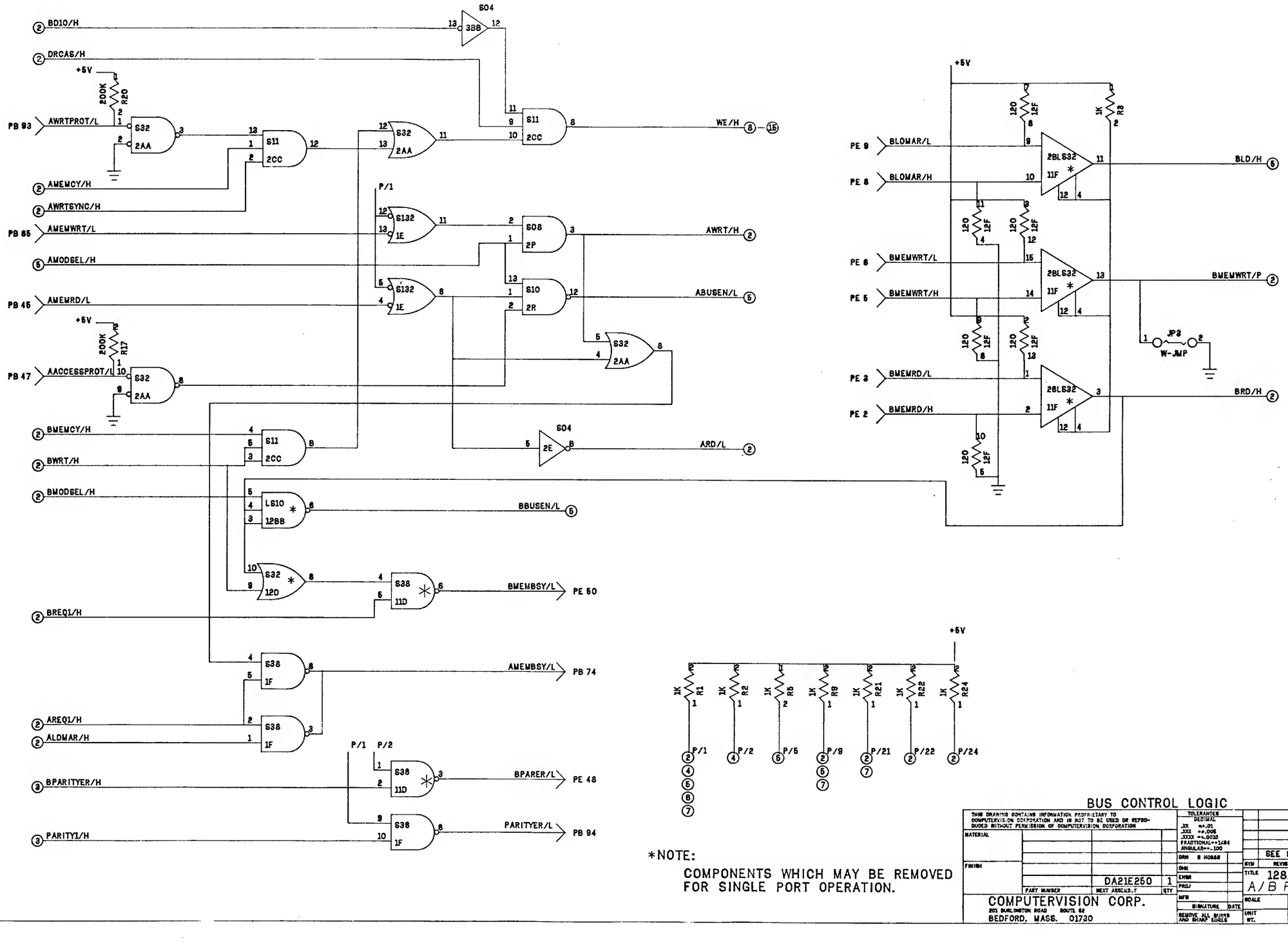
SCALE

DWG NO. DS21E252

UNIT WT.

SHT 2 OF 14 SHTS


ABUS0/H
BBUS0/H
ABUS1/H
BBUS1/H
ABUS2/H
BBUS2/H
ABUS3/H
BBUS3/H
S157
5E
D-IN0
D-IN1
D-IN2
D-IN3
ABUS4/H
BBUS4/H
ABUS5/H
BBUS5/H
ABUS6/H
BBUS6/H
ABUS7/H
BBUS7/H
8E
O-IN4
D-IN5
D-IN8
D-IN7
ABUS8/H
BBUS8/H
ABUS9/H
BBUS8/H
ABUS10/H
BBUS10/H
ABUS11/H
BBUS11/H
7E
D-IN8
D-IN9
D-IN10
D-IN11
ABUS12/H
BBUS12/H
ABUS13/H
BBUS13/H
ABUS14/H
BBUS14/H
ABUS15/H
BBUS15/H
6E
D-IN12
D-IN13
D-IN14
D-IN15
BMEM1/H
DRCAS/H
AWRTSYNC/L
AMEM1/H
PARITYERR/H
BWRT/L
BMEM1/H
BRST+BCLR/L
AIORST/L
S08
10CC
10C
12P
2P
S04
12C
74LS74
11C
APARITY
BPARITY
LED1
LED2
+5V
PARITY1/H
BPARITYER/H
BPARITYER/L
O-OUT0
O-OUT1
O-OUT2
D-OUT3
D-OUT4
D-OUT5
D-OUT6
O-OUT7
D-OUT8
D-OUT9
D-OUT10
D-OUT11
D-OUT12
D-OUT13
D-OUT14
D-OUT15
LS378
12M
12L
2M
2L
B-MOD0
B-MOD1
B-MOD2
B-MOD3
B-MOD4
B-MOD5
B-MOD6
B-MOD7
B-MOD8
B-MOD9
B-MOD10
B-MOD11
B-MOD12
B-MOD13
B-MOD14
B-MOD15
A-MOD0
A-MOD1
A-MOD2
A-MOD3
A-MOD4
A-MOD5
A-MOD6
A-MOD7
A-MOD8
A-MOD9
A-MOD10
A-MOD11
A-MOD12
A-MOD13
A-MOD14
A-MOD15
INVPAR/L
O-IN0
D-IN1
O-IN2
D-IN3
O-IN4
D-IN5
D-IN8
D-IN7
S280
10E
9E
11M
11L
1K
RP4
S51
10D
PARITY-IN
PARITY-OUT
D-OUT0
D-OUT1
D-OUT2
D-OUT3
D-OUT4
D-OUT5
D-OUT6
D-OUT7
D-OUT8
D-OUT9
D-OUT10
D-OUT11
D-OUT12
D-OUT13
D-OUT14
D-OUT15
PARITYERR/H
DS21E252
E
*NOTE:
COMPONENTS WHICH MAY BE REMOVED
FOR SINGLE PORT OPERATION.
DATA IN MUX,DATA OUT LATCH,PARITY LOGIC
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION
MATERIAL
FINISH
PART NUMBER
DA21E250
NEXT ASSEMBLY
QTY
1
TOLERANCES
DECIMAL
XX ±.01
XXX ±.005
XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100
DRN
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
COMPUTERVISION CORP.
203 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
SEE SHT. 1
SYM
REVISION DESCRIPTION
CHK
APPD
DATE
TITLE
128/32K MEMORY
A/B PORT SCH DIA
SCALE
DWG NO. DS21E252
UNIT WT.
SHT 3 OF 16 SHTS



*NOTE:
COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

DS21E252
E

BUS CONTROL LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL
FINISH
PART NUMBER: DA21E250 1
NEXT ASSY: QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
.XX ±=.01
.XXX ±=.005
.XXXX ±=.0010
FRACTIONAL=±1/64
ANGULAR=±=.100

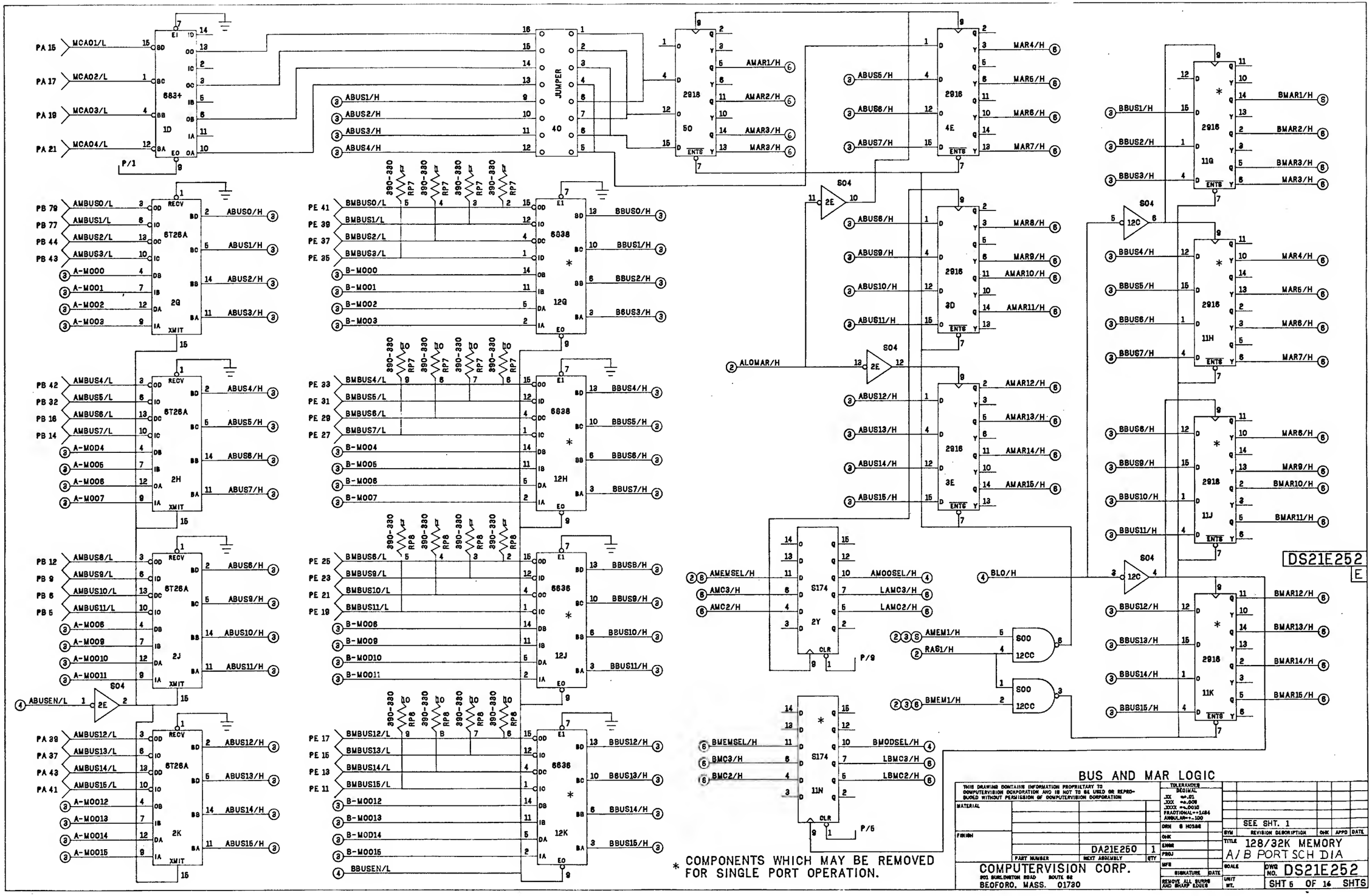
DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 4 OF 16 SHTS



BUS AND MAR LOGIC
* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
DA21E250
128/32K MEMORY
A/B PORT SCH DIA
DWG NO. DS21E252
SHT 5 OF 16 SHTS
DS21E252
E

STANDARD JUMPERS (FOR OTHER CONFIGS. SEE SHT. 1)

128K MEM . CPU JP9, JP10, JP11, JP12, JP13, JP14

128K MEM . DIST MODE - JP9, JP10, JP11, JP13, JP15, JP16

ADDR MUX CONTROL	
A	B	RAM ADDR
L	L	CAS ADDR
H	L	APORT RAS ADDR
L	H	BPORT RAS ADDR
H	H	REFRESH ADDR

2X AND 2Y TO BE ADDED FOR FUTURE EXPANSION

* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

APORT/BPORT SELECT, ADDR MUX, REFRESH CNTR, RAS CLOCK

DS21E252 E

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL			
FINISH			
	DA21E250	1	
	PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES UNLESS XX ±.01, XXX ±.005, XXXX ±.0010, FRACTIONAL ±1/64, ANGULAR ±.100

DRN B MOSS

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY A/B PORT SCHDIA

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 8 OF 16 SHTS

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

PA B4 ADS5/L
PA B2 ADS4/L
PA 46 ADS3/L
PA 66 ADS2/L
PA 6B ADS1/L
PA 72 ADS0/L
P6 41 ARQENB/L
PA 9B AINTPIN/L
PA 52 A6TRT/H
PA 5D ACLR/H
PE 42 RESET/H
PA 74 AIDPLS/H
PA 7D IORST/H
PA 4D AINTA/H
PC 11 6IORST/H
PC 13 6CLR/H
PC 15 BIDPLS/H
PC 25 BDSD/L
PC 23 6DS1/L
PC 21 BDS2/L
PC 19 BDS3/L
PC 31 BRQEN6/L
PD 1 6INTPIN/L
PA 94 DCHPIN/L
DCHPOUT/L PA 93
AINTPDUT/L PA 95
AINTR/L PB 29
6PARITYER/L
6INTR/L PC 1
PD 2
6INTOUT/L PC 5D
6DATA7/L PC 45
AIORST/L
6DATA6/L PC 43
6DATA5/L PC 41
6RST+6CLR/L
6DATA4/L PC 39
BDATA1/L PC 37
BPDRTACT/L PC 5
ADATA15/L PB 55
ADATA13/L PB 64
ADATA11/L PB 5B
6PINH6/H
INVPAR/L
PWRST/L
6DXSD/L
6DXS1/L
6DXS2/L
6DXS3/L
BDXSD/L
BDXS1/L
BDXS2/L
BDXS3/L
6PARITYER/H
JP5 W-JMP
JP8 W-JMP
12S SWITCH
11X SWITCH
1U 8834
2U 93S47
16 8834
12X 8834
12Y 8834
A=B
A=6
LS04
LS74 1P
LS74 11AA
SD4 11V
SD6 12P
SDB 2P
S11E 11B6
LS11 2N
LS11 2S
S74 1B6
1R FILT
12AA FILT
LS11 2N
S1D 2R
S10 2R
LS11 2S
LS10 12B6
LS10 12B6
611 11B6
36 1N
38 12V
36 12U
36 1Q
+5V
R32 1K
R19 390
R14 1K
R41 390 Ω
R40 390 Ω
R7 330
R8 390
R18 330
RP12 260-162

* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

I/O LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES DECIMAL XX ±.01 XXX ±.005 XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY QTY 1

DRN S HOGGS

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND BREAK EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/ 32K MEMORY A/B PORT SCHEM. DIAGRAM

SCALE

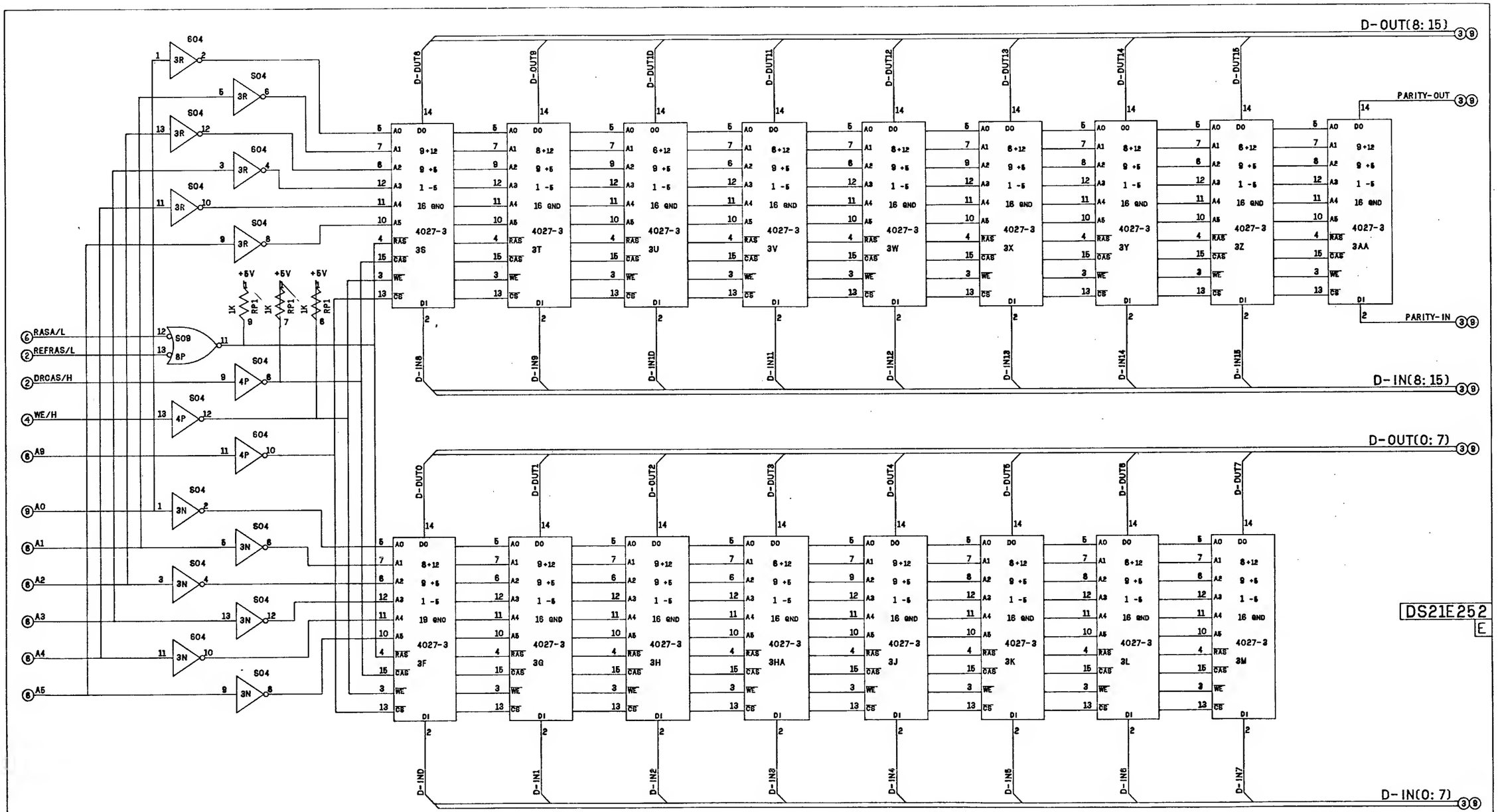
DWG NO. DS21E252

UNIT WT.

SHT 7 OF 16 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 0173D

DS21E252 E



MEMORY CHIPS 3S THRU 3AA AND 3F THRU 3M MAY BE EITHER ALL 4027-3 OR 4116-3 PARTS

DS21E252 E

MEMORY ROW A

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES DECIMAL XX ±.01 XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.1DG

MATERIAL

FINISH

DRN B HOBBS

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

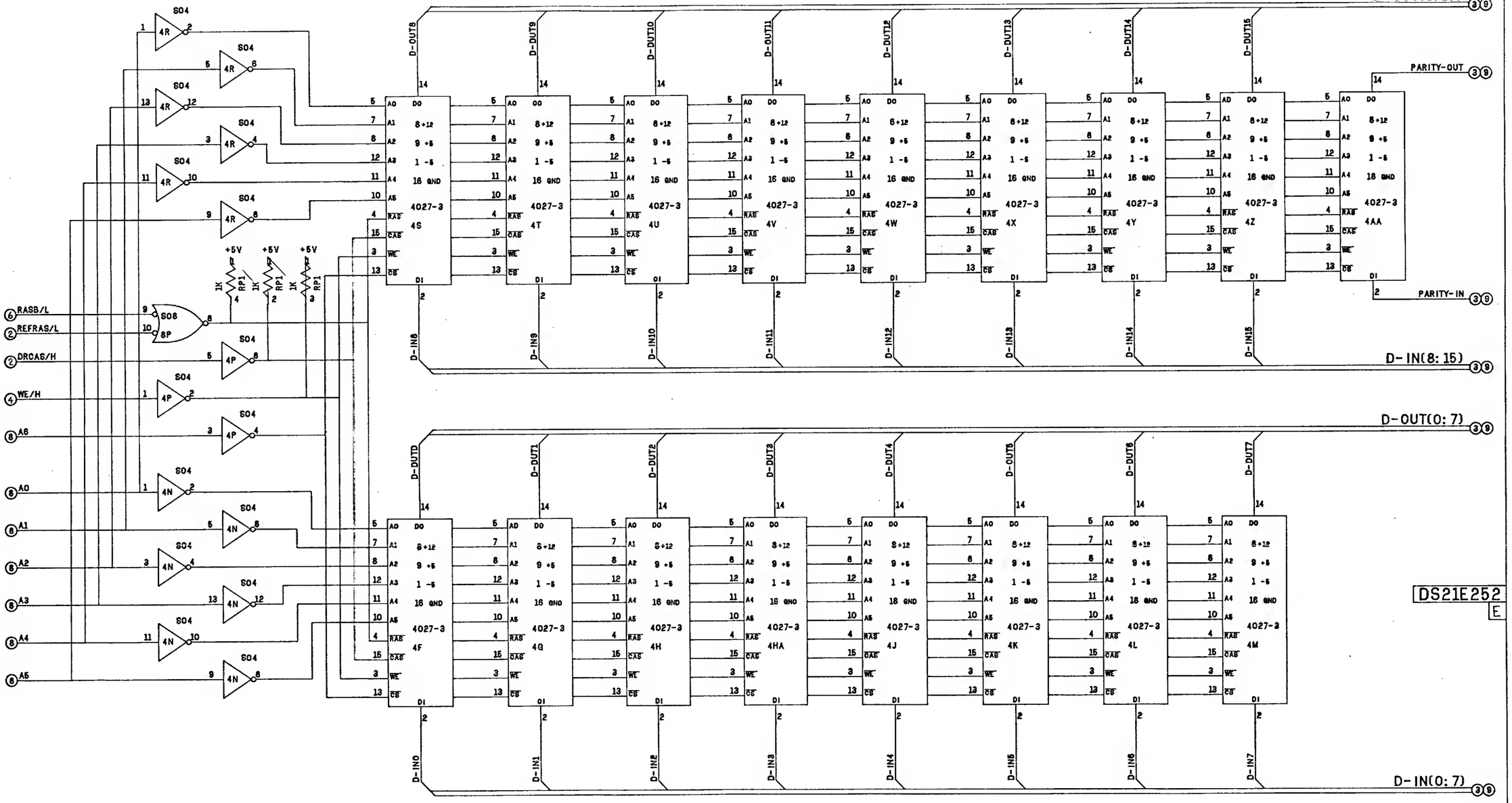
TITLE 128/32K MEMORY A/B PORT SCHEM. DIAGRAM

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 9 OF 16 SHTS



MEMORY CHIPS 4S THRU 4AA
AND 4F THRU 4M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW B

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL

FINISH

PART NUMBER	NEXT ASSEMBLY	QTY
	DA21E250	1

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
.XX =±.01
.XXX =±.005
.XXXX =±.0010
FRACTIONAL=±1/64
ANGULAR=±.100

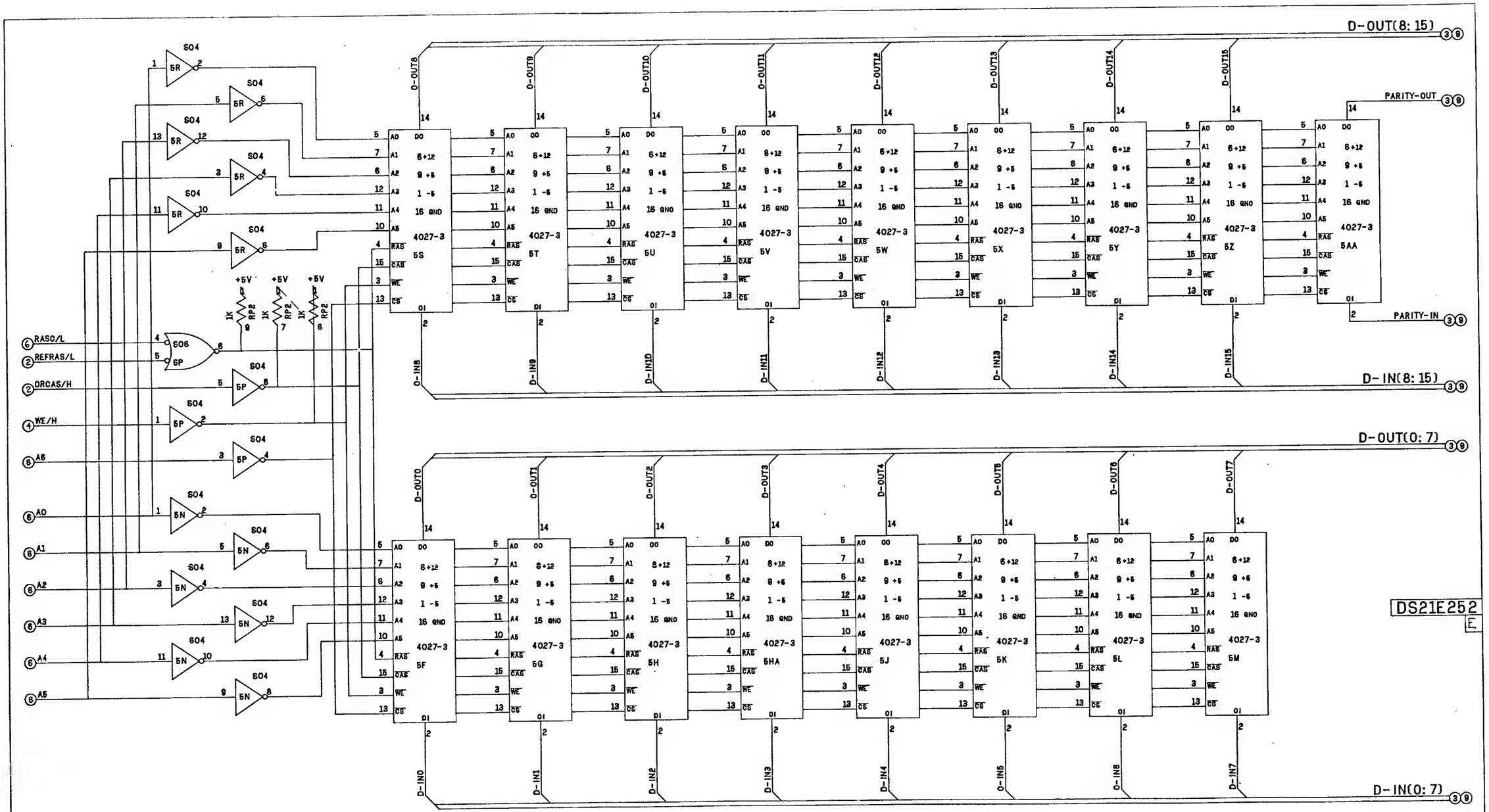
DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 9 OF 16 SHTS



DS21E252
E

MEMORY CHIPS 5S THRU 5AA
AND 5F THRU 5M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW C

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY QTY 1

TOLERANCES DECIMAL
XX ±.01
XXX ±.005
XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.30

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
801 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

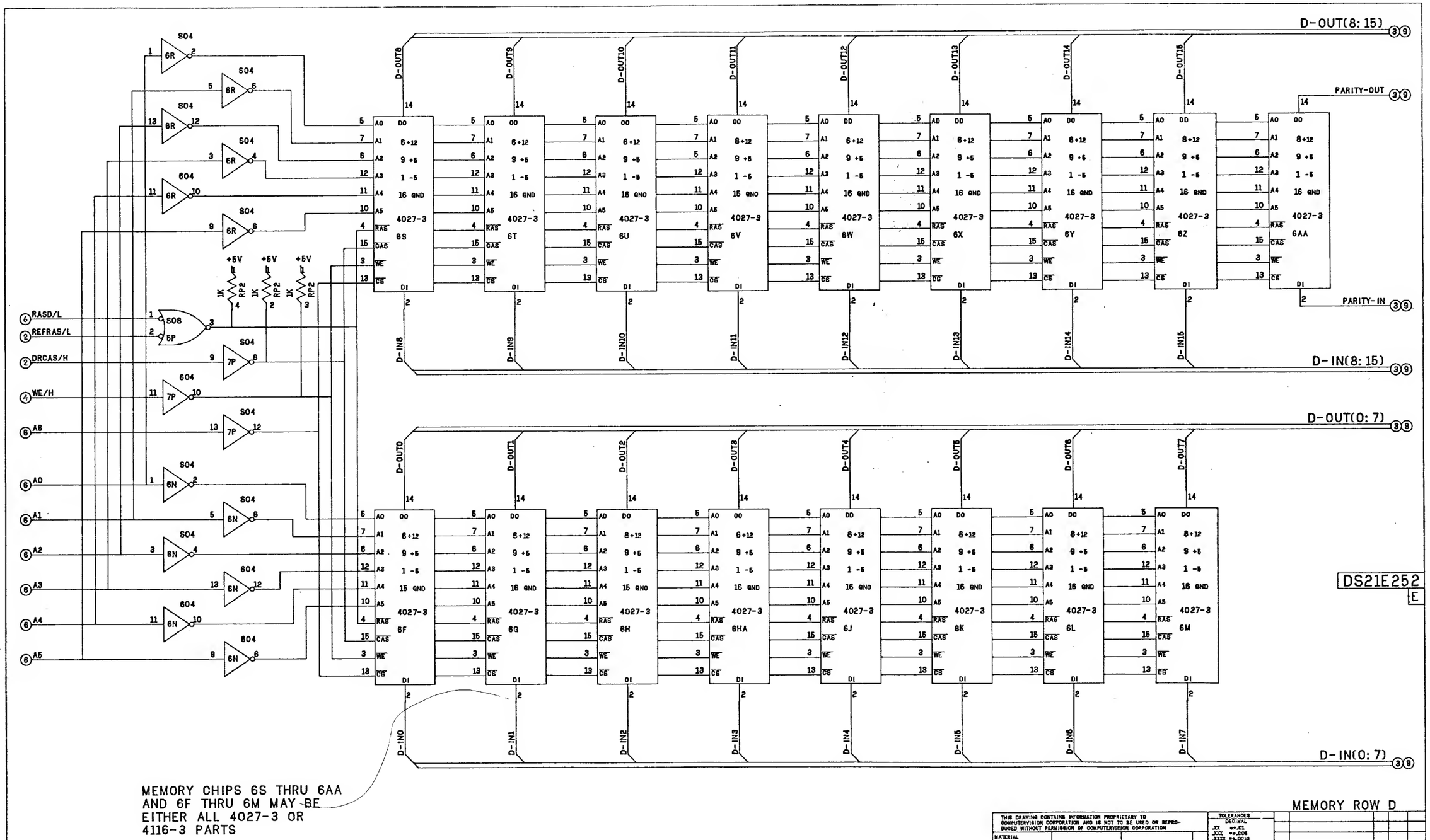
TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE

DWG NO. DS21E252

LIMIT WT.

SHT 10 OF 16 SHTS



MEMORY ROW D

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL

FINISH

PART NUMBER	NEXT ASSEMBLY	QTY
	DA21E250	1

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
.XX =±.01
.XXX =±.005
.XXXX =±.0010
FRACTIONAL=±1/64
ANGULAR=±.100

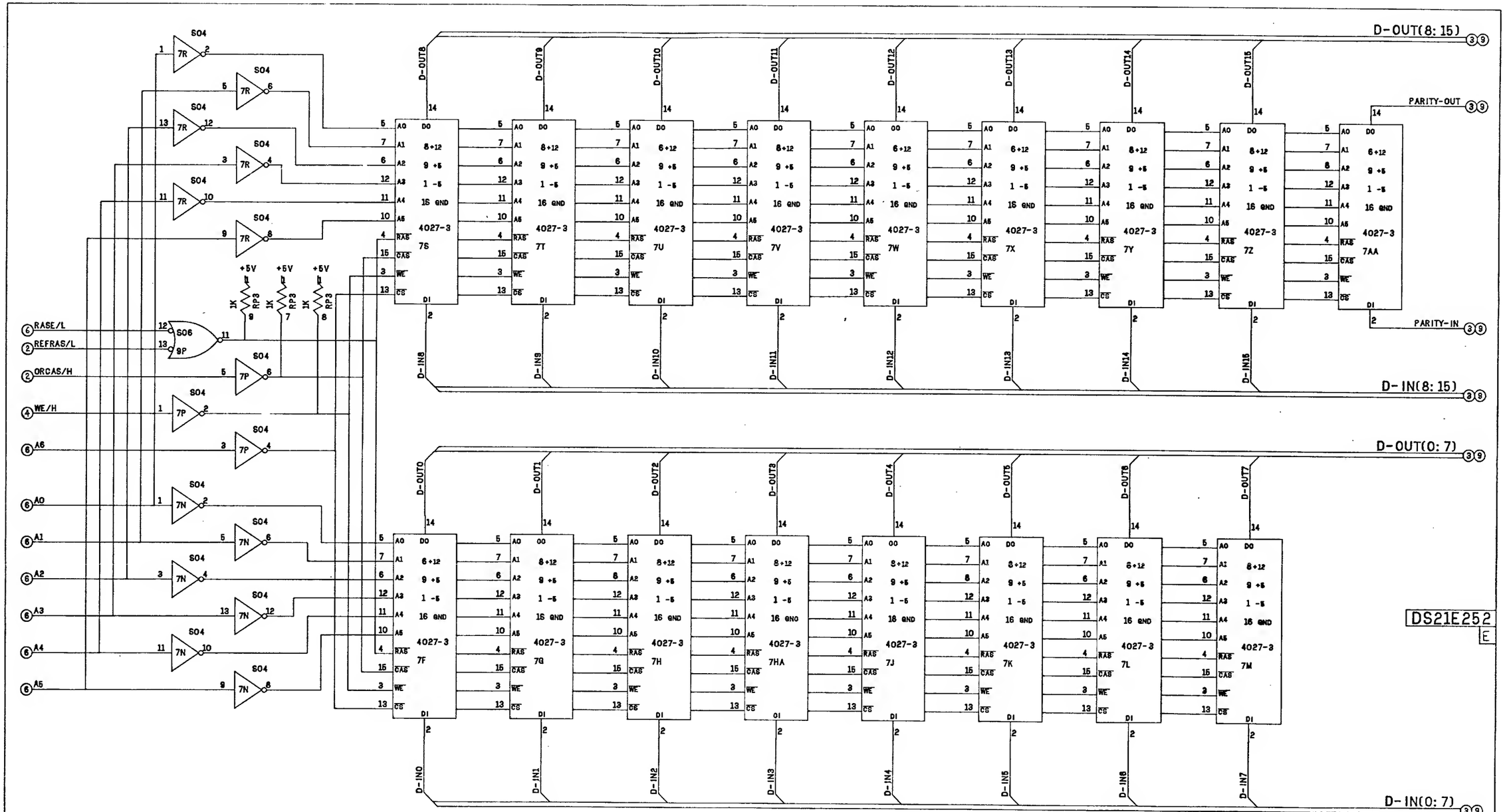
DRN S HOBBS
CHK
ENGR
PROJ
MFR
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE
UNIT WT.
DWG NO. DS21E252
SHT 11 OF 16 SHTS



MEMORY CHIPS 7S THRU 7AA
AND 7F THRU 7M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
XX ±.01
XXX ±.005
XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.30

DRN B MOSBE
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

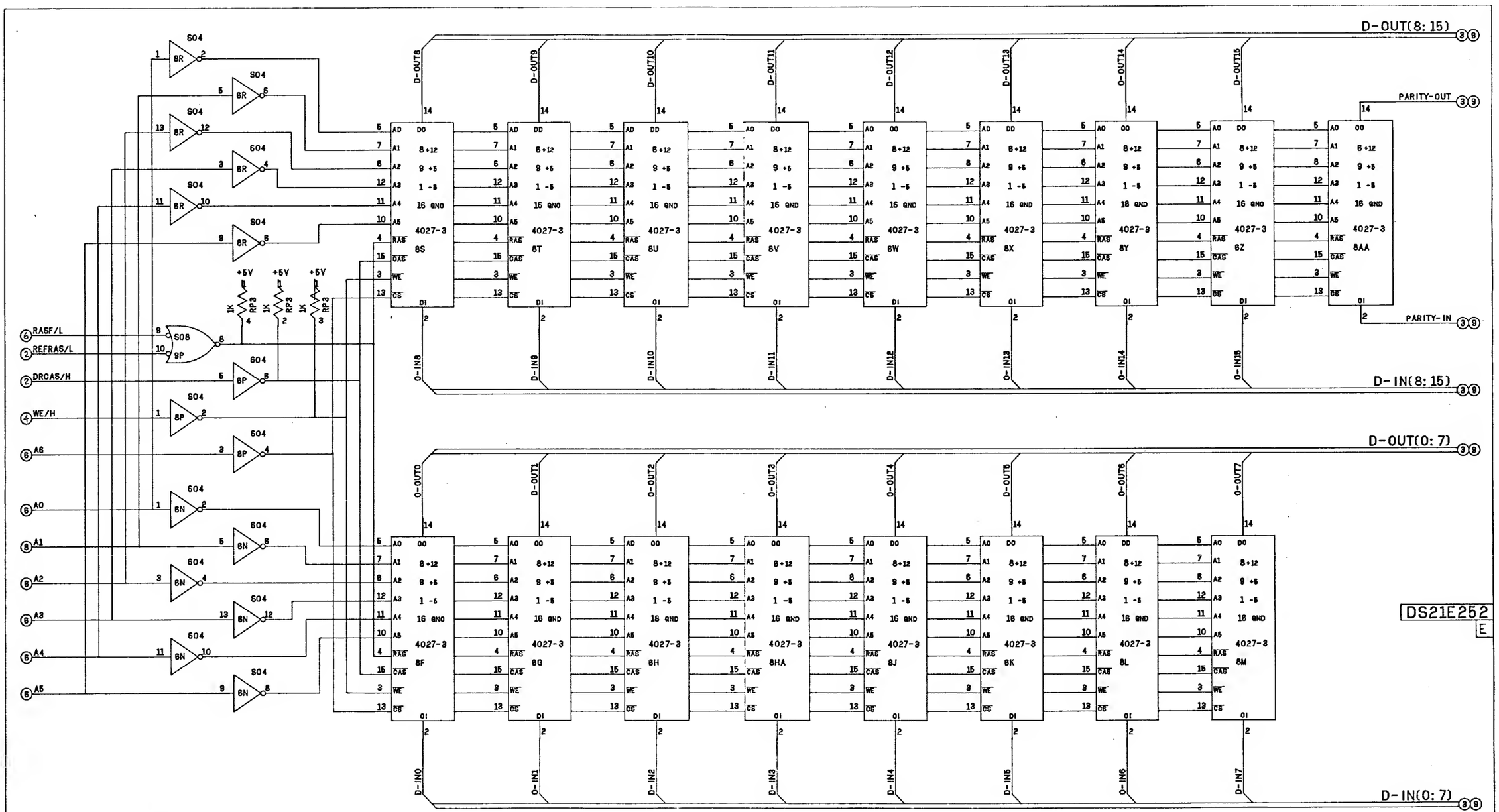
MEMORY ROW E

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 12 OF 14 SHTS



MEMORY CHIPS 8S THRU 8AA
AND 8F THRU 8M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

MEMORY ROW F

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES
DECIMAL
.XX +/-.01
.XXX +/-.005
.XXXX +/-.0050
FRACTIONAL +/-1/64
ANGULAR +/-.10

MATERIAL
FINISH
PART NUMBER: DA21E250
NEXT ASSEMBLY
QTY: 1

DRN B HOBBS
CHK
ENGR
PROJ
MFR
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

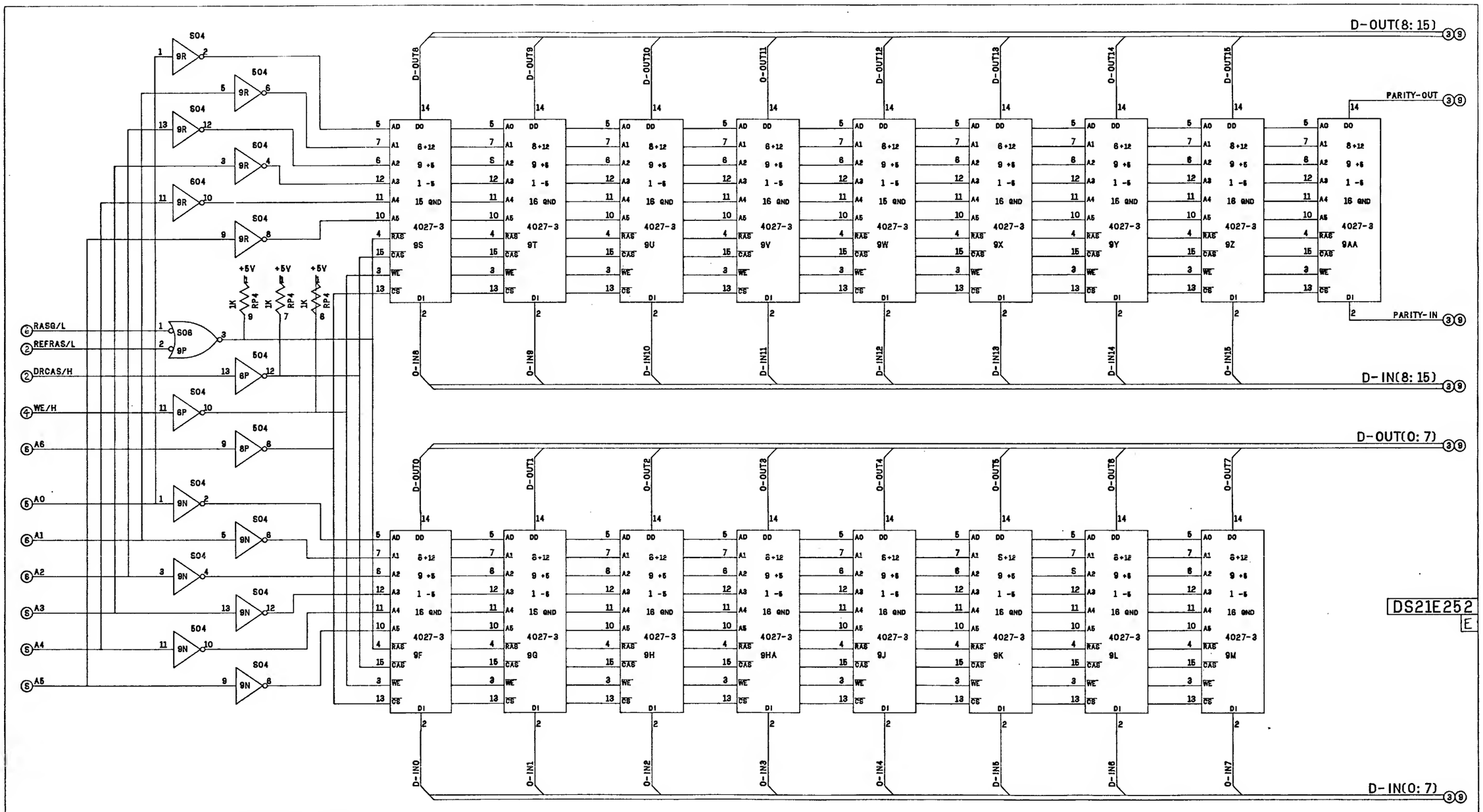
SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 13 OF 16 SHTS

COMPUTERVISION CORP.
300 BURLINGTON RD. ROUTE 62
BEDFORD, MASS. 01730



MEMORY CHIPS 9S THRU 9AA
AND 9F THRU 9M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW G

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

TOLERANCES DECIMAL
XX ±.01
XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100

DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A7,B PORT SCHDIA.

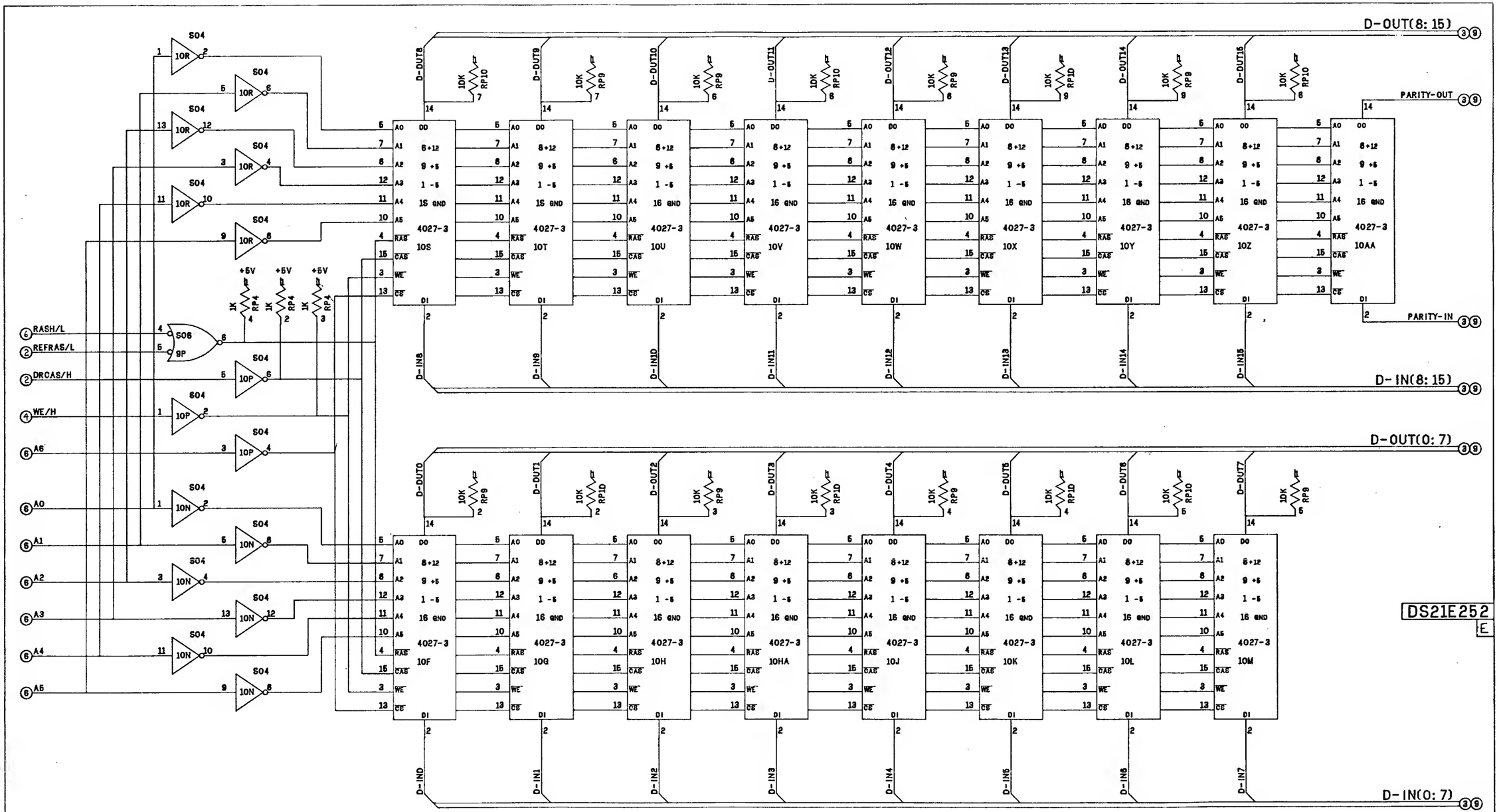
SCALE

DWG NO. DS21E252

UNIT WT.

SHT 14 OF 16 SHTS

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730



MEMORY CHIPS 10S THRU 10AA
AND 10F THRU 10M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

MEMORY ROW H

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE DISCLOSED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL			
FINISH			
	DA21E250	1	
	PART NUMBER	NEXT ASSEMBLY	QTY

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
XX ±0.01
XXX ±0.005
XXXX ±0.0030
FRACTIONAL ±1/64
ANGULAR ±0.500

DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
	SEE SHT. 1			

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 15 OF 16 SHTS

B PORT CONNECTORS

CONN C

1	$\overline{\text{BINTR}}$		2
3			4
5	$\overline{\text{BPORTACT}}$		6
7			8
9			10
11	BIORST		12
13	BCLR		14
15	BIOPLS		16
17			18
18	$\overline{\text{BDS 3}}$		20
21	$\overline{\text{BDS 2}}$		22
23	$\overline{\text{BDS 1}}$		24
25	$\overline{\text{BDS 0}}$		28
27			28
29			30
31	$\overline{\text{BRQENB}}$		32
33			34
35	$\overline{\text{BDATA 10}}$		36
37	$\overline{\text{BDATA 1}}$		38
38	$\overline{\text{BDATA 4}}$		40
41	$\overline{\text{BDATA 5}}$		42
43	$\overline{\text{BDATA 6}}$		44
45	$\overline{\text{BDATA 7}}$		46
47	FREE		48
49		$\overline{\text{BINTPOUT}}$	50

CONN E

1		B MEM RD	2
3	$\overline{\text{B MEM RO}}$		4
5	B MEMWRT	$\overline{\text{BMEMWRT}}$	6
7		BLDMAR	8
9	$\overline{\text{BLDMAR}}$		10
11	$\overline{\text{B MEM BUS 15}}$		12
13	$\overline{\text{B MEM BUS 14}}$		14
15	$\overline{\text{B MEM BUS 13}}$		16
17	$\overline{\text{B MEM BUS 12}}$		18
18	$\overline{\text{B MEM BUS 11}}$		20
21	$\overline{\text{B MEM BUS 10}}$		22
23	$\overline{\text{B MEM BUS 9}}$		24
25	$\overline{\text{B MEM BUS 8}}$		26
27	$\overline{\text{B MEM BUS 7}}$		28
29	$\overline{\text{B MEM BUS 6}}$		30
31	$\overline{\text{B MEM BUS 5}}$		32
33	$\overline{\text{B MEM BUS 4}}$		34
35	$\overline{\text{B MEM BUS 3}}$		36
37	$\overline{\text{B MEM BUS 2}}$	$\overline{\text{BMAD2}}$	38
39	$\overline{\text{B MEM BUS 1}}$	$\overline{\text{BMAD1}}$	40
41	$\overline{\text{B MEM BUS 0}}$	$\overline{\text{RESET}}$	42
43	$\overline{\text{BMC 3}}$	$\overline{\text{BMADO}}$	44
45	$\overline{\text{BMC 2}}$	$\overline{\text{BMCO}}$	46
47	$\overline{\text{BMC 1}}$	$\overline{\text{BPARER}}$	48
48		$\overline{\text{B MEM BUSY}}$	50

ALL UNUSED PINS GROUNDED

VOLTAGE FEEDS FOR CONNECTORS PA,PB	
+12 VOLTS	B46,A7,A8
-5 VOLTS	B81
-12 VOLTS	B71,B72
+5 VOLTS	A/B3,A/B4,A/B97,A/B98
GND	A/B1,A/B2,A/B99,A/B100

DS21E252
E

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

TOLERANCES
DECIMAL
XX ±0.01
XXX ±0.005
.XXXX ±0.0050
FRACTIONAL ±1/64
ANGULAR ±0.100

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 16 OF 16 SHTS

32K/128K Memory Unit
DS21E227 (Obsolete)

	Sheet No.
Block Diagram	
Address Selection	1
B Port Connections	1
Data Input/Output	2
Bus and MAR Logic	3
Cycle Timing Logic	4
Refresh Logic	4
Bus Control Logic	5
I/O Logic	6
Typical Rank	7
Memory Address Logic	8
Array	9

128K BOARD (DA21E225-01)

I. JUMPER INFO.
(CONNECTIONS NORMALLY MADE IN ETCH)

1. JP3
2. JP5
3. JP7
4. JP1

II. ADDRESS SELECT CHART

* FIELD #	$\overline{MC\emptyset}$	$\overline{MC1}$	CLOSED CONTACTS SWITCH PACK 1T
0, 1, 2, 3	H	H	2, 4 * *
4, 5, 6, 7	H	L	2, 3 * *
8, 9, 10, 11	L	H	1, 4 * *
12, 13, 14, 15	L	L	1, 3 * *

* NOTE: EACH FIELD # REPRESENTS ONE 32K SEGMENT OF MEMORY.

* * NOTE: ALL OTHER CONTACTS OPEN.

III. HARDWARE CONFIGURATION INFO.

1. MEMORY CHIPS ARE MK4116-3.
2. RESISTORS R2 & R3 ARE BOTH INSERTED.
3. ADJUST POT 1 (R138) SUCH THAT TP4H-4 HAS A REPITITION RATE OF 14.5 μs.

GENERAL NOTES :

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, ±5%
   CAPACITOR VALUES ARE IN MICROFARADS

32K BOARD (DA21E225-02)

I. JUMPER INFO.

1. CUT CONNECTIONS JP3, JP5, JP7, JP1
2. MAKE CONNECTIONS JP2, JP4, JP 6,

II. ADDRESS SELECT CHART

* FIELD #	$\overline{MC\emptyset}$	$\overline{MC1}$	$\overline{MC2}$	$\overline{MC3}$	CLOSED CONTACTS SWITCH PACK 1T
0	H	H	H	H	2, 4, 6, 8 * *
1	H	H	H	L	2, 4, 6, 7 * *
2	H	H	L	H	2, 4, 5, 8 * *
3	H	H	L	L	2, 4, 5, 7
4	H	L	H	H	2, 3, 6, 8
5	H	L	H	L	2, 3, 6, 7
6	H	L	L	H	2, 3, 5, 8
7	H	L	L	L	2, 3, 5, 7
8	L	H	H	H	1, 4, 6, 8
9	L	H	H	L	1, 4, 6, 7
10	L	H	L	H	1, 4, 5, 8
11	L	H	L	L	1, 4, 5, 7
12	L	L	H	H	1, 3, 6, 8
13	L	L	H	L	1, 3, 6, 7 * *
14	L	L	L	H	1, 3, 5, 8 * *
15	L	L	L	L	1, 3, 5, 7 * *

* NOTE: EACH FIELD # REPRESENTS ONE 32K SEGMENT OF MEMORY.

* * NOTE: ALL OTHER CONTACTS OPEN

III. HARDWARE CONFIGURATION INFO.

1. MEMORY CHIPS ARE MK4027-3.
2. REMOVE RESISTOR R2.
3. ADJUST POT 1 (R138) SUCH THAT TP4H-4 HAS REPITITION RATE OF 29 μs.

DS21E227

B PORT CONNECTORS

CONN D

1	BINTPOUT		
11	BIORST		
	BCLR		
	BIOPLS		
	BINTA		
	$\overline{BDS5}$		
21	$\overline{BDS4}$		
	$\overline{BDS3}$		
	$\overline{BDS2}$		
	$\overline{BDS1}$		
	$\overline{BDS\emptyset}$		
31	$\overline{BRQENB}$		
	BDATAI0		
	BDATAI1		
	BDATAI2		
41	BDATAI3		
	BDATAI4		
	BDATAI5		
49	$\overline{BINTR}$		50

CONN E

1	B MEM RD		
	B MEM WRT		
	B ACCESSPROT		
	B WRT PROT		
	B MEM BUSY		
11	B MEM BUS 15		
			$\overline{14}$
			$\overline{13}$
			$\overline{12}$
			$\overline{11}$
21			$\overline{10}$
			$\overline{9}$
			$\overline{8}$
			$\overline{7}$
			$\overline{6}$
31			$\overline{5}$
			$\overline{4}$
			$\overline{3}$
			$\overline{2}$
			$\overline{1}$
41	B MEM BUS $\emptyset$		
	$\overline{B\ MC3}$		
	$\overline{B\ MC2}$		
	$\overline{B\ MC1}$	B PARITY ER	
49	$\overline{B\ MC\emptyset}$	BLD MAR	50

ALL UNUSED PINS GROUNDED

VOLTAGE FEEDS FOR CONNECTORS PA, PB	
+12 VOLTS	B46, A7, A8
−5 VOLTS	B81 A5, A6
−12 VOLTS	B71, B72
+5 VOLTS	A/B3, A/B4, A/B97, A/B98
GND	A/B1, A/B2, A/B99, A/B100

DS21E227 C

OBSOLETE per eng DR 21E250

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL: —

FINISH: —

PART NUMBER: DA21E225 | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'

DRN —
CHK —
ENGR —
PROJ —
MFG —
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

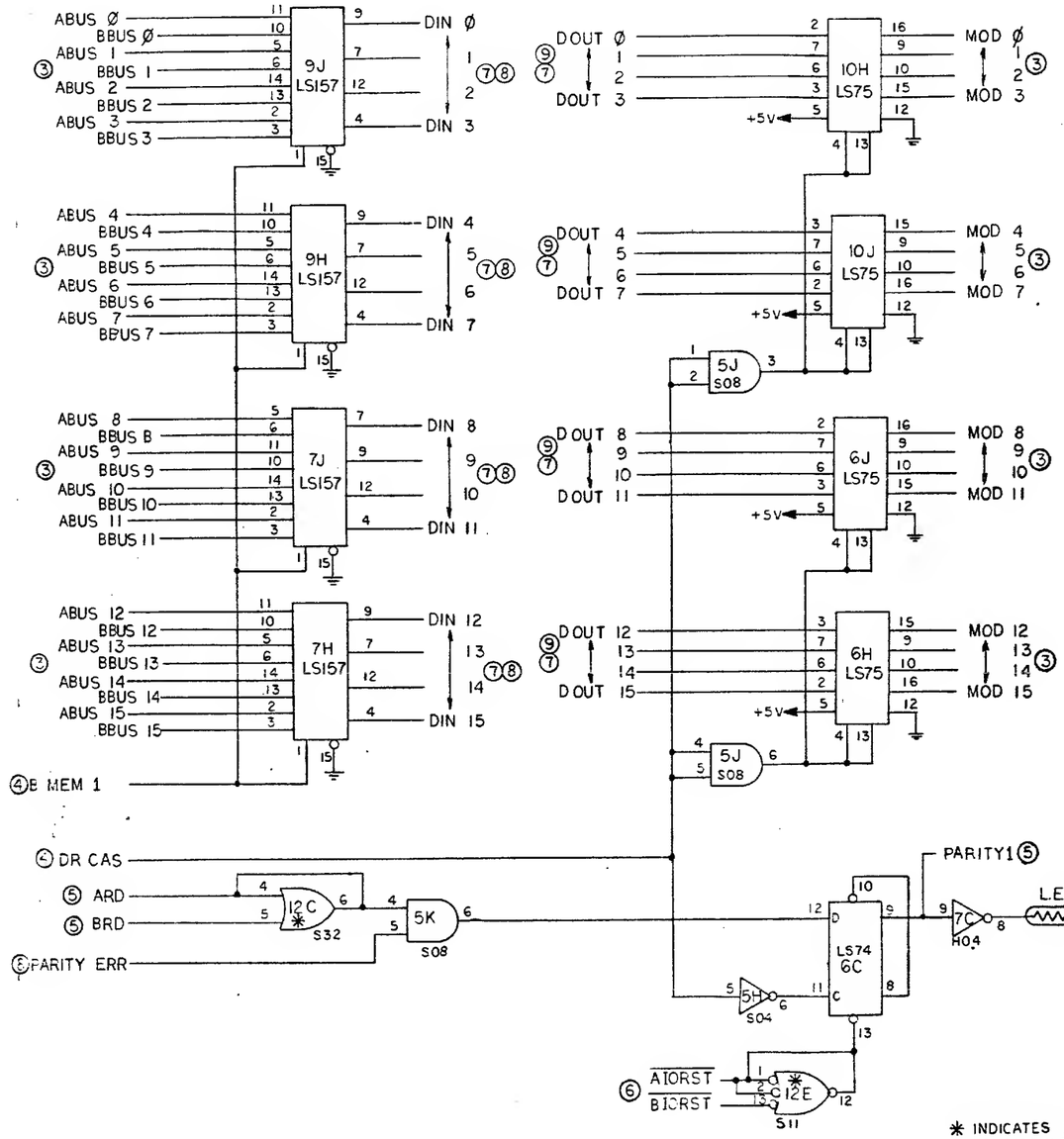
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	ECO # 2963			1/17
B	ECO # 2935			10/16
A	REL ECO 2849			8/16

TITLE: 128K/32K MEMORY SCHEMATIC

SCALE: —
DWG NO. DS21E227
UNIT WT. —
SHEET 1 OF 9 SHEETS

MAKEPEACE P-3000



✱ INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.

DS21E227 C

DATA INPUT / OUTPUT LOGIC

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MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY
	SEE SH. 1	

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN 7/78
CHK 7/78
ENGR 8/78
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SH. 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE 128K/32K MEMORY SCHEMATIC

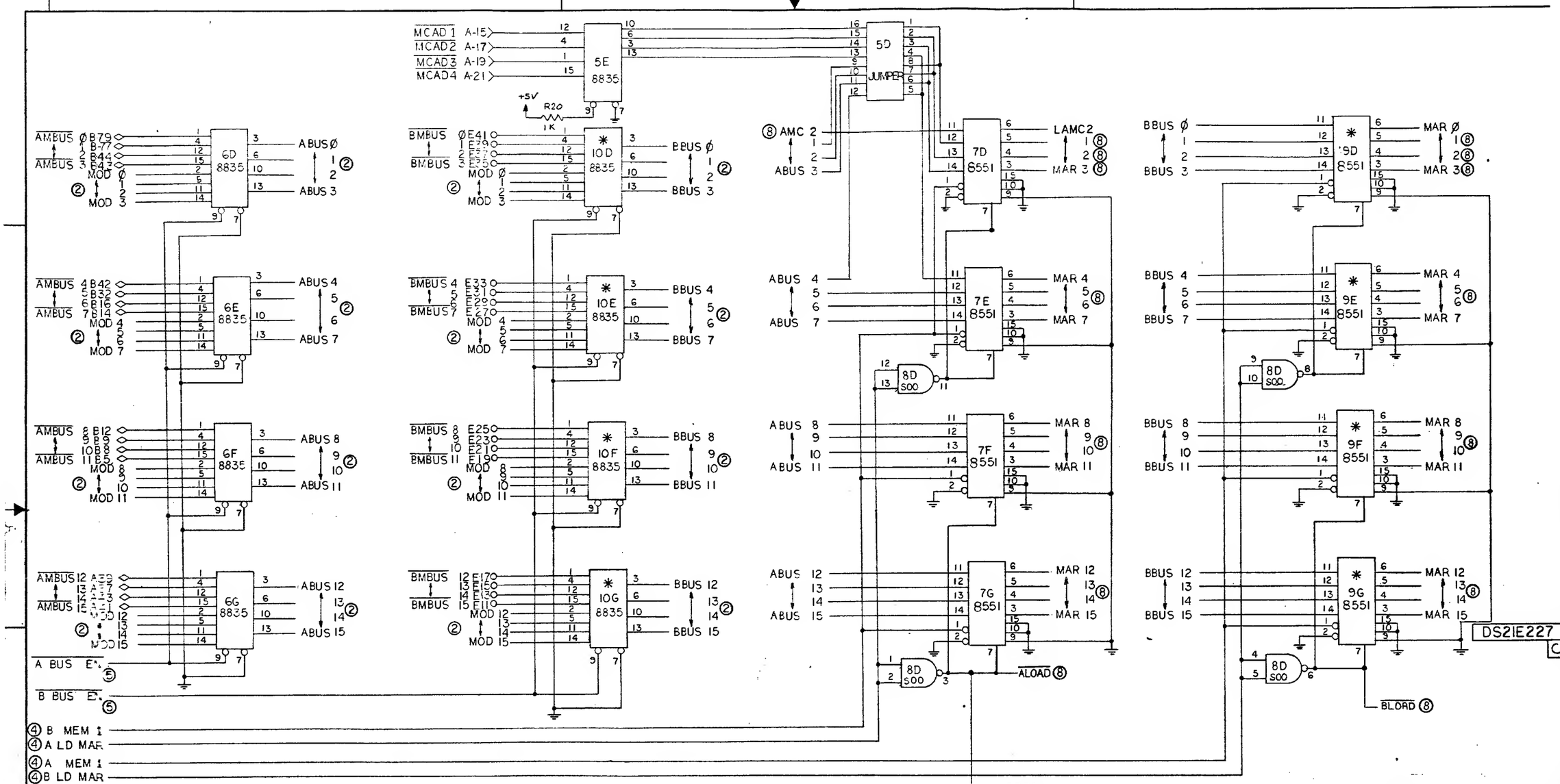
SCALE

DWG NO. DS21E227

UNIT WT.

SHEET 2 OF 9 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



5D JUMPER PLUG	
MUC OPERATION	1,16 2,15 3,14 4,13
NON MUC OPERATION	5,12 6,11 7,10 8,9

* INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.

BUS & MAR LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY
	SEE SHT 1	

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN 7/72
CHK 7/24
ENGR 8/72
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT.1		

TITLE 128K/32K MEMORY SCHEMATIC

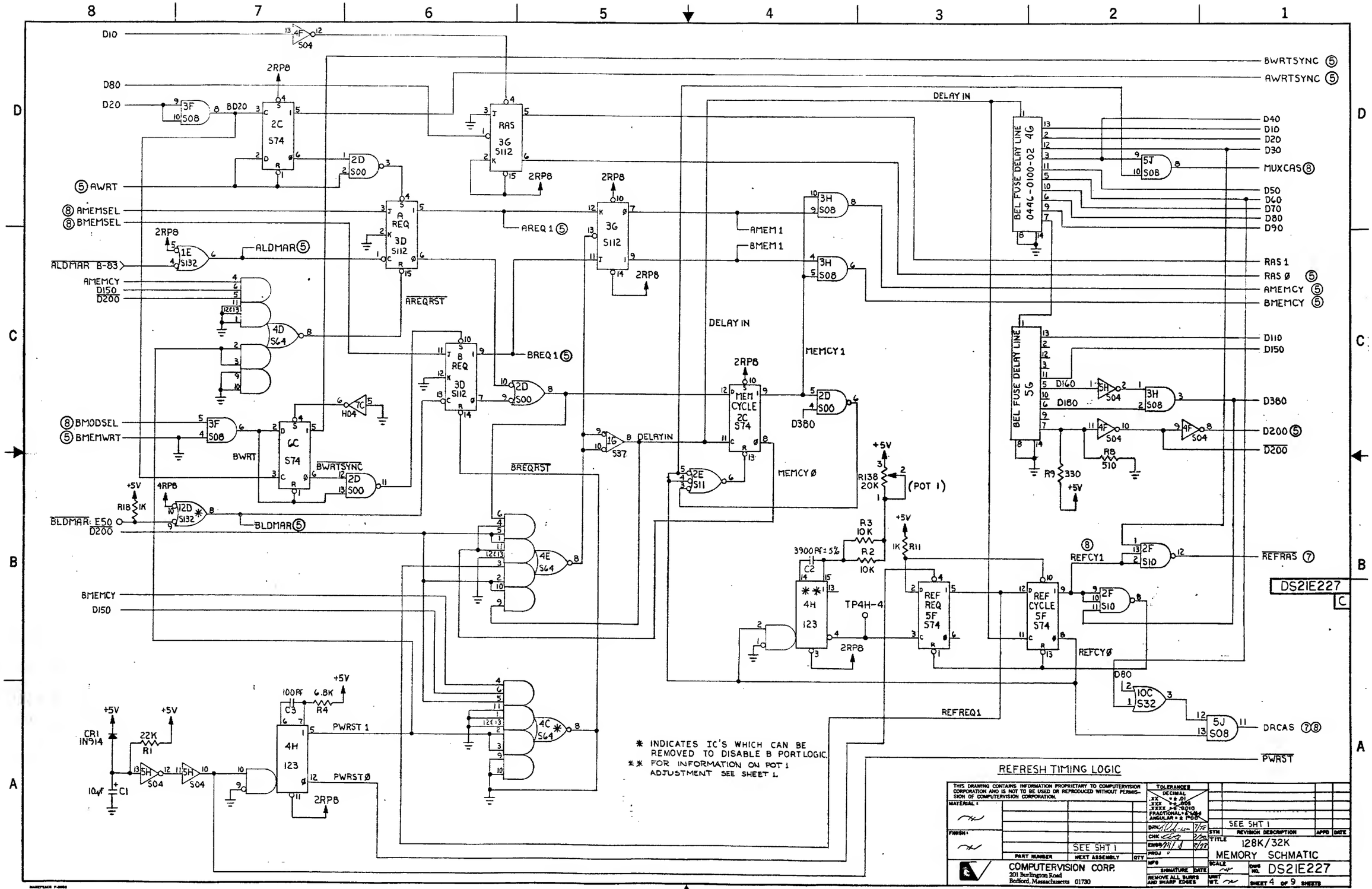
SCALE

DWG NO. DS21E227

UNIT WT.

SHEET 3 OF 9 SHEETS

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803



* INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.
** FOR INFORMATION ON POT 1 ADJUSTMENT SEE SHEET 1.

REFRESH TIMING LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY
SEE SHT 1

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN 7/78
CHK 7/78
ENGR 7/78
PROJ
MFG
SIGNATURE | DATE
REMOVE ALL BURRS AND SHARP EDGES

SYM | REVISION DESCRIPTION | APPD | DATE
SEE SHT 1

TITLE 128K/32K MEMORY SCHMATIC

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

SCALE
UNIT WT.
DWG NO. DS21E227
SHEET 4 OF 9 SHEETS

8 7 6 5 4 3 2 1

D C B A

BMEMWRT E3
④D200
④DRCAS
⑧AMODSEL
AWRTPROT B93
④AMEMCY
④AWRTSYNC
AMEMWRT B85
④BWRTSYNC
⑧BMODSEL
AMEMRD B45
AACCESSPROT B47
④BMEMCY
BWRTPROT E7
BMEMRD E1
BACCESSPROT E5
②PARITY1
④ALDMAR
④BWRT
④AREQ1
④BREQ1
④BLDMAR

1F S32 · 2E S11 · 1F S32 · 1E S132 · 1E S132 · 1E S132 · 1F S32 · 12E S11 · 12C S32 · 12D S132 · 12C S32 · 1F S32 · 12C S32 · 1C S38 · 1C S38 · 5C S38 · 5C S38

4RP8 · 2RP8 · 2RP8 · 4PR8

ARD/AWRT · BRD/BWRT · ARD ② · BRD ② · B/WRITE · AWRT

12D S132 · 2E S11 · 3F S08 · 2F S10 · 11E S10 · 5C S38 · 1C S38 · 1C S38

+5V R14 1K · +5V R13 1K

BMEMWRT ④
WE ⑦⑧
ABUSEN ③
BBUSEN ③
E48 BPARITYER
B94 PARITYER
B74 AMEMBSY
E9 BMEMBSY

DS21E227 C

✱ INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.

BUS CONTROL LOGIC

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MATERIAL · FINISH · PART NUMBER · NEXT ASSEMBLY · QTY · SEE SHT 1

TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 1°00'

DRN · CHK · ENGR · PROJ · MFG · SIGNATURE · DATE

REMOVE ALL BURRS AND SHARP EDGES

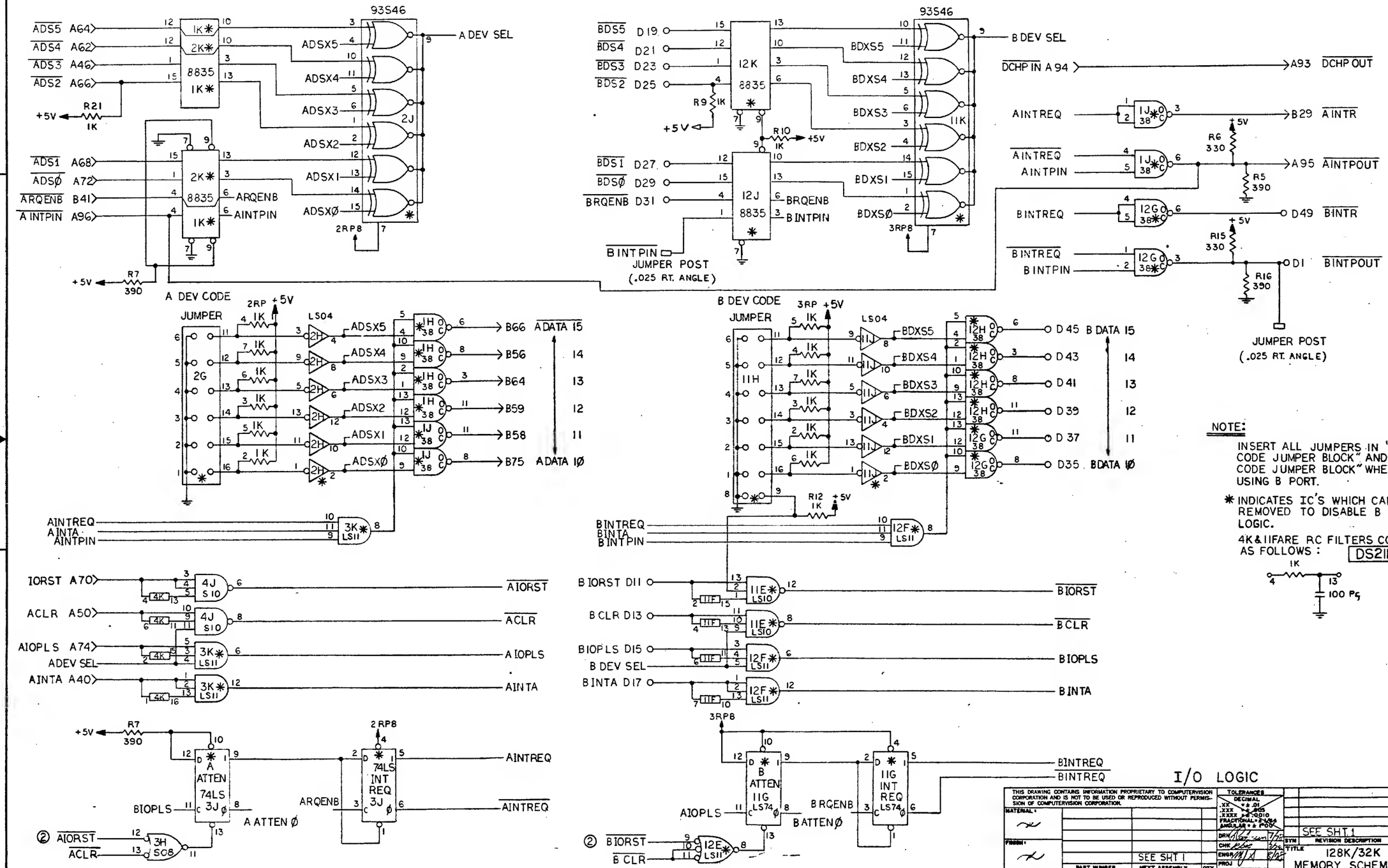
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

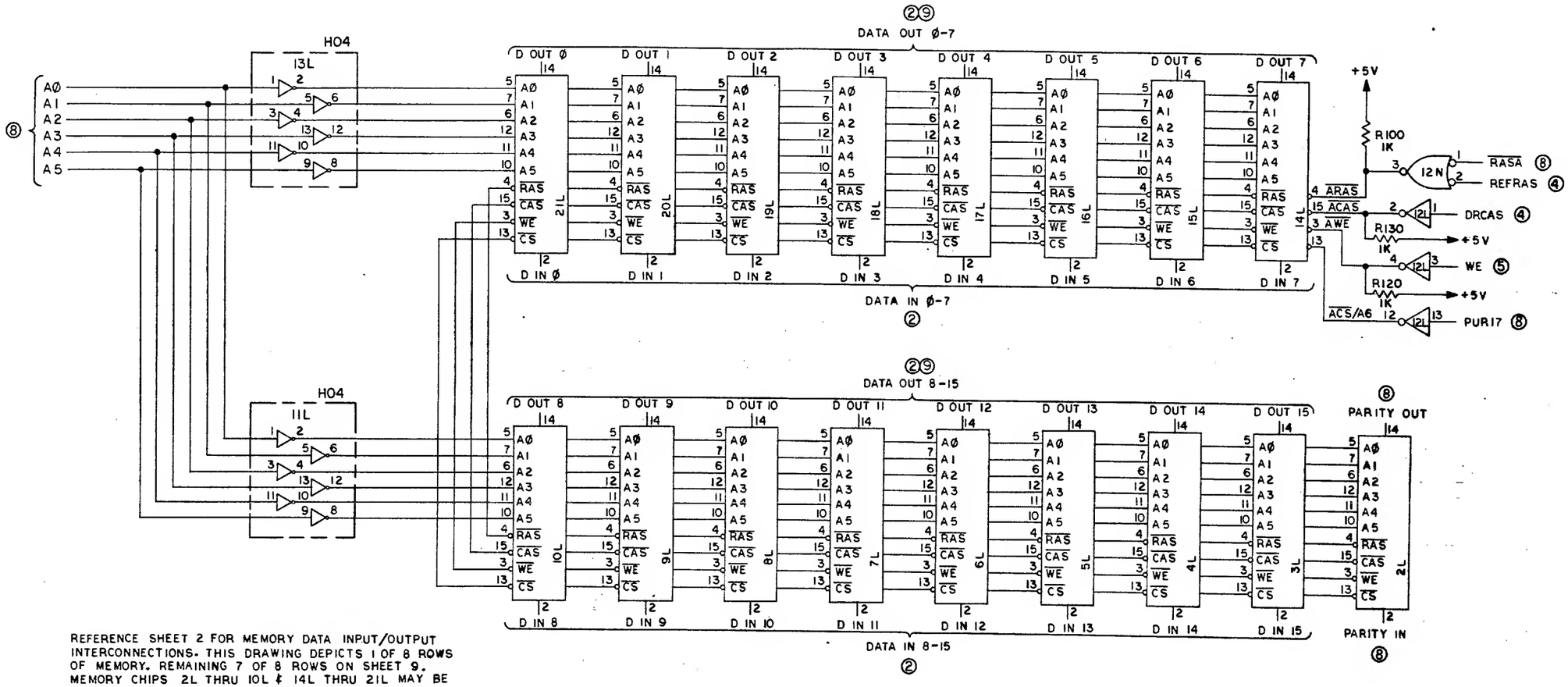
SEE SHT 1

SYM	REVISION DESCRIPTION	APPD	DATE

TITLE 128K/32K MEMORY SCHEMATIC

SCALE NONE · DWG NO. DS21E227 · UNIT WT. · SHEET 5 OF 9 SHEETS


93S46
ADS5 A64
ADS4 A62
ADS3 A46
ADS2 A66
+5V
R21
1K
1K*
2K*
8835
1K*
ADSX5
ADSX4
ADSX3
ADSX2
ADSX1
ADSXØ
2J
2RP8
ADS1 A68
ADSØ A72
ARQENB B41
AINTPIN A96
2K*
8835
1K*
ARQENB
AINTPIN
+5V
R7
390
A DEV SEL
93S46
BDS5 D19
BDS4 D21
BDS3 D23
BDS2 D25
R9 1K
+5V
12K
8835
R10
1K
+5V
BDS1 D27
BDSØ D29
BRQENB D31
BINTPIN
JUMPER POST
(.025 RT. ANGLE)
12J
8835
BRQENB
BINTPIN
BDXS5
BDXS4
BDXS3
BDXS2
BDXS1
BDXSØ
11K
3RP8
B DEV SEL
DCHP IN A 94
A93 DCHP OUT
AINTREQ
B29 AINTR
AINTREQ
AINTPIN
RG
330
+5V
R5
390
A95 AINTPOUT
BINTREQ
D49 BINTR
BINTREQ
BINTPIN
RI5
330
+5V
RI6
390
D1 BINTPOUT
JUMPER POST
(.025 RT. ANGLE)
A DEV CODE
JUMPER
2RP +5V
2G
LS04
ADSX5
ADSX4
ADSX3
ADSX2
ADSX1
ADSXØ
B66 ADATA 15
B56 14
B64 13
B59 12
B58 11
B75 ADATA IØ
AINTREQ
AINTA
AINTPIN
3K*
LS11
B DEV CODE
JUMPER
3RP +5V
11H
LS04
BDXS5
BDXS4
BDXS3
BDXS2
BDXS1
BDXSØ
D 45 B DATA 15
D 43 14
D 41 13
D 39 12
D 37 11
D35 BDATA IØ
BINTREQ
BINTA
BINTPIN
12F*
LS11
IORST A70
ACLR A50
AIOPLS A74
ADEV SEL
AINTA A40
4K
4J
S10
3K*
LS11
AIORST
ACLR
AIOPLS
AINTA
BIORST DII
BCLR DI3
BIOPLS DI5
B DEV SEL
BINTA DI7
11E*
LS10
12F*
LS11
BIORST
BCLR
BIOPLS
BINTA
+5V
R7
390
2RP8
A
ATTEN
74LS
3J Ø
74LS
INT
REQ
3J Ø
AIOPLS
ARQENB
AINTREQ
AINTREQ
A ATTEN Ø
② AIORST
ACLR
3H
S08
3RP8
B
ATTEN
IIG
LS74 Ø
IIG
INT
REQ
LS74 Ø
BIOPLS
BRQENB
BINTREQ
BINTREQ
B ATTEN Ø
② BIORST
B CLR
12E*
LS11
NOTE:
INSERT ALL JUMPERS IN "A DEV CODE JUMPER BLOCK" AND "B DEV CODE JUMPER BLOCK" WHEN NOT USING B PORT.
* INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.
4K & IIFARE RC FILTERS CONNECTED AS FOLLOWS :
1K
100 PF
I/O LOGIC
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
TOLERANCES
DECIMAL
FRACTIONAL ± 1/64
ANGULAR ± 5 POST
MATERIAL
FINISH
PART NUMBER
NEXT ASSEMBLY
QTY
SEE SHT 1
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
REMOVE ALL BURRS AND SHARP EDGES
SIGNATURE DATE
DRN
CHK
ENGR
PROJ
MFG
SYM REVISION DESCRIPTION APPD DATE
SEE SHT 1
TITLE
128K/32K
MEMORY SCHEMATIC
SCALE NONE
DWG NO. DS21E227
SHEET WT.
SHEET 6 OF 9 SHEETS
DS21E227
C



REFERENCE SHEET 2 FOR MEMORY DATA INPUT/OUTPUT INTERCONNECTIONS. THIS DRAWING DEPICTS 1 OF 8 ROWS OF MEMORY. REMAINING 7 OF 8 ROWS ON SHEET 9. MEMORY CHIPS 2L THRU 10L & 14L THRU 21L MAY BE 4027-3 OR 4116-3

DS21E227
C

TYPICAL MEMORY ROW

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL
FINISH
SEE SH. 1
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00'
REMOVE ALL BURRS AND SHARP EDGES

DRN | CHK | ENGR | PROJ | MFG | SIGNATURE | DATE

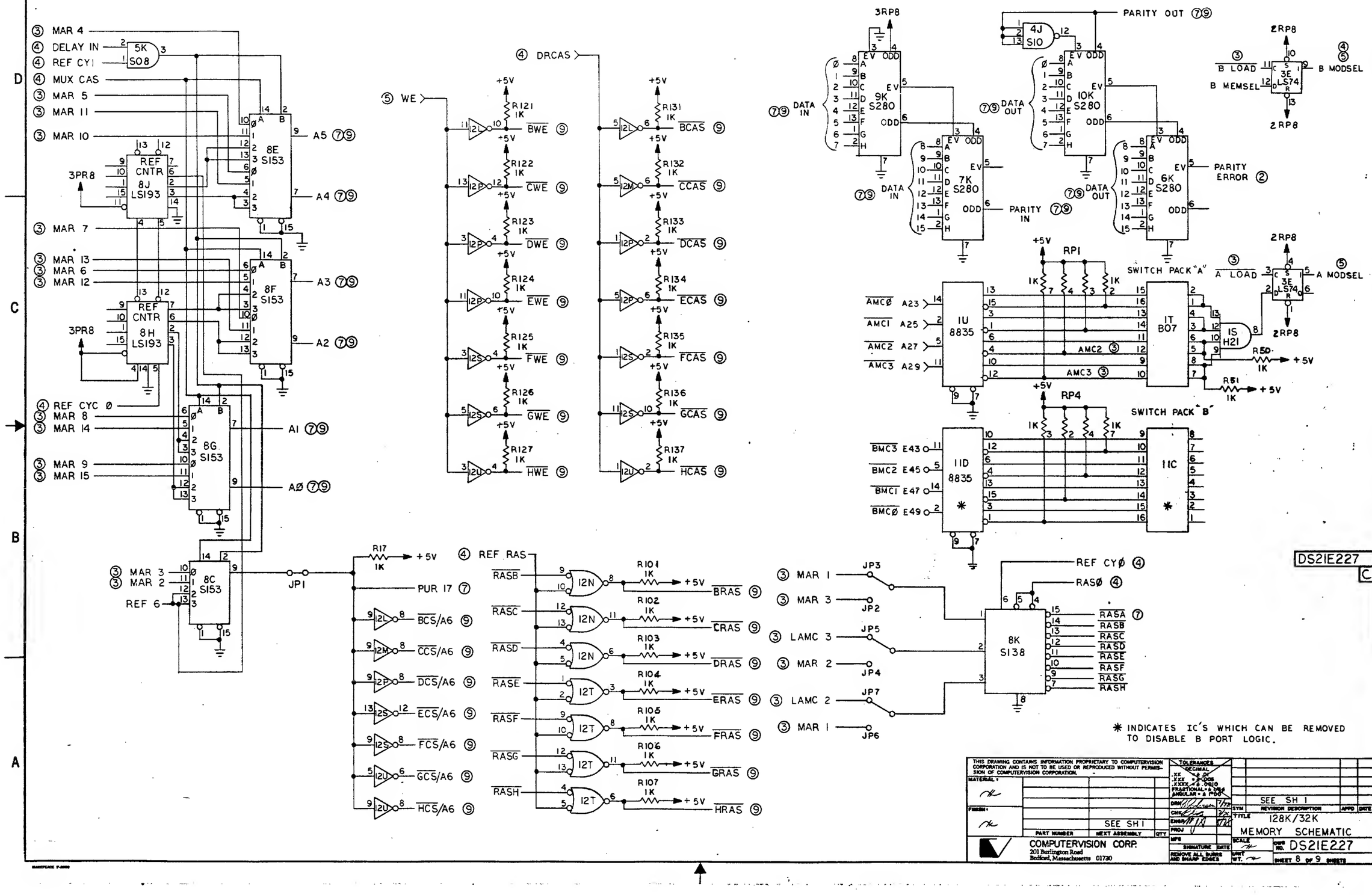
SEE SH. 1
SYM | REVISION DESCRIPTION | APPD | DATE

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

TITLE
128K/32K
MEMORY SCHEMATIC

SCALE | DWG NO. DS21E227

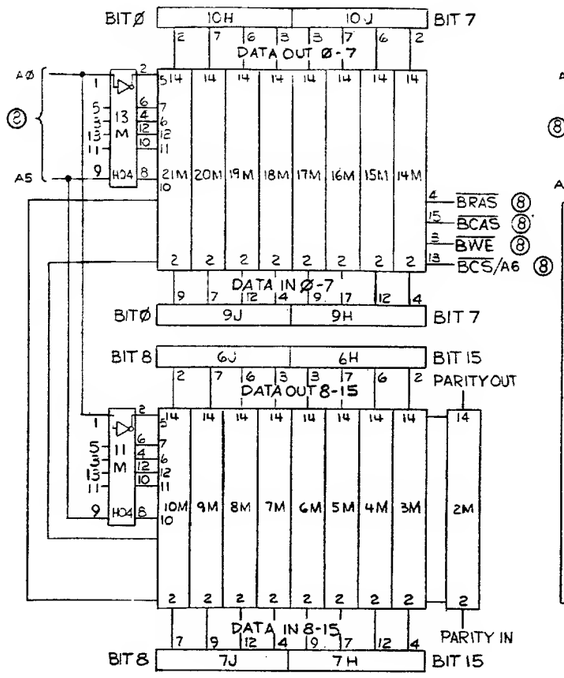
SHEET WT. | SHEET 7 OF 9 SHEETS

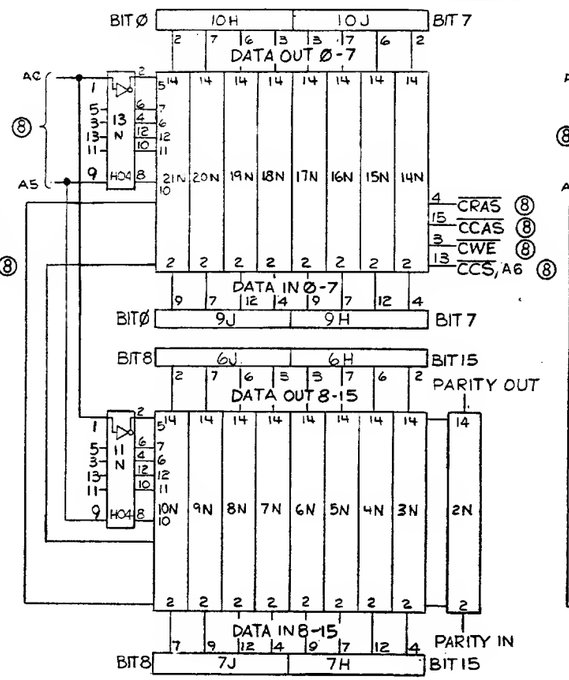

8
7
6
5
4
3
2
1
D
C
B
A
③ MAR 4
④ DELAY IN
④ REF CYI
④ MUX CAS
③ MAR 5
③ MAR 11
③ MAR 10
③ MAR 7
③ MAR 13
③ MAR 6
③ MAR 12
④ REF CYC Ø
③ MAR 8
③ MAR 14
③ MAR 9
③ MAR 15
③ MAR 3
③ MAR 2
REF 6
5K S08
3PR8
REF CNTR 8J LS193
REF CNTR 8H LS193
8E S153
8F S153
8G S153
8C S153
A5 ⑦⑨
A4 ⑦⑨
A3 ⑦⑨
A2 ⑦⑨
A1 ⑦⑨
AØ ⑦⑨
JP1
⑤ WE
④ DRCAS
R121 1K
R122 1K
R123 1K
R124 1K
R125 1K
R126 1K
R127 1K
R131 1K
R132 1K
R133 1K
R134 1K
R135 1K
R136 1K
R137 1K
BWE ⑨
CWE ⑨
DWE ⑨
EWE ⑨
FWE ⑨
GWE ⑨
HWE ⑨
BCAS ⑨
CCAS ⑨
DCAS ⑨
ECAS ⑨
FCAS ⑨
GCAS ⑨
HCAS ⑨
⑦⑨ DATA IN
⑦⑨ DATA OUT
9K S280
10K S280
7K S280
6K S280
PARITY OUT ⑦⑨
PARITY IN ⑦⑨
PARITY ERROR ②
4J S10
3RP8
2RP8
3E LS74
B LOAD ③
B MEMSEL
B MODSEL ④⑤
A LOAD ③
A MODSEL ⑤
SWITCH PACK "A"
SWITCH PACK "B"
RP1
RP4
1K
AMCØ A23
AMC1 A25
AMC2 A27
AMC3 A29
BMC3 E43
BMC2 E45
BMC1 E47
BMCØ E49
1U 8835
1D 8835
1T B07
1S H21
1C
1K
R50 1K
R51 1K
+5V
AMC2 ③
AMC3 ③
REF CYØ ④
RASØ ④
8K S138
RASA ⑦
RASB
RASC
RASD
RASE
RASF
RASG
RASH
R17 1K
PUR 17 ⑦
BCS/A6 ⑨
CCS/A6 ⑨
DCS/A6 ⑨
ECS/A6 ⑨
FCS/A6 ⑨
GCS/A6 ⑨
HCS/A6 ⑨
④ REF RAS
R101 1K
R102 1K
R103 1K
R104 1K
R105 1K
R106 1K
R107 1K
BRAS ⑨
CRAS ⑨
DRAS ⑨
ERAS ⑨
FRAS ⑨
GRAS ⑨
HRAS ⑨
③ MAR 1
③ MAR 3
③ LAMC 3
③ MAR 2
③ LAMC 2
③ MAR 1
JP3
JP2
JP5
JP4
JP7
JP6
DS21E227
C
✱ INDICATES IC'S WHICH CAN BE REMOVED TO DISABLE B PORT LOGIC.
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
TOLERANCES DECIMAL
MATERIAL
FINISH
SEE SH 1
PART NUMBER
NEXT ASSEMBLY
QTY
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730
REMOVE ALL BURRS AND SHARP EDGES
SIGNATURE
DATE
SCALE
SIZE C
DWG NO. DS21E227
SHEET 8 OF 9 SHEETS
SYM
REVISION DESCRIPTION
APPD
DATE
TITLE
128K/32K
MEMORY SCHEMATIC

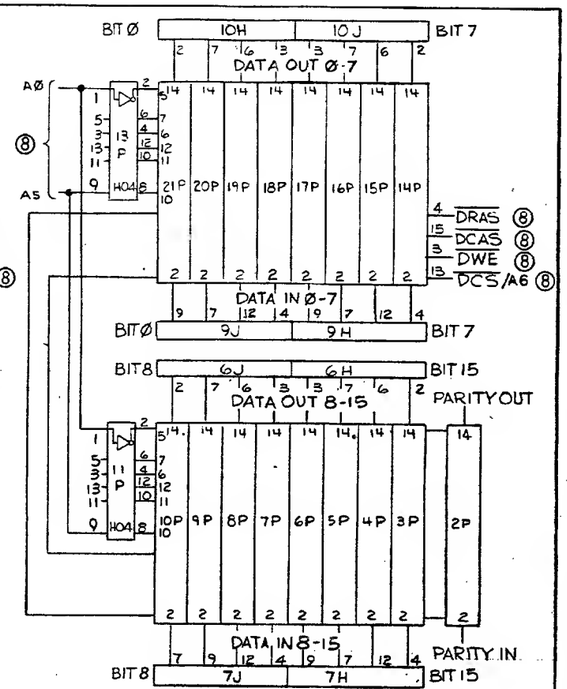
MEMORY ARRAY

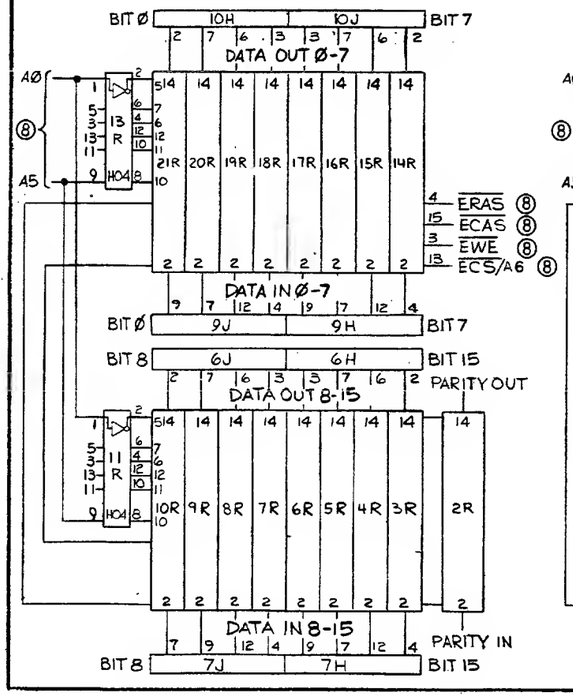
FOR MORE DETAIL OF TYPICAL MEMORY SEE SHEET 7
FOR MEMORY DATA INPUT/OUTPUT INTERCONNECTIONS, SEE SHEET 2

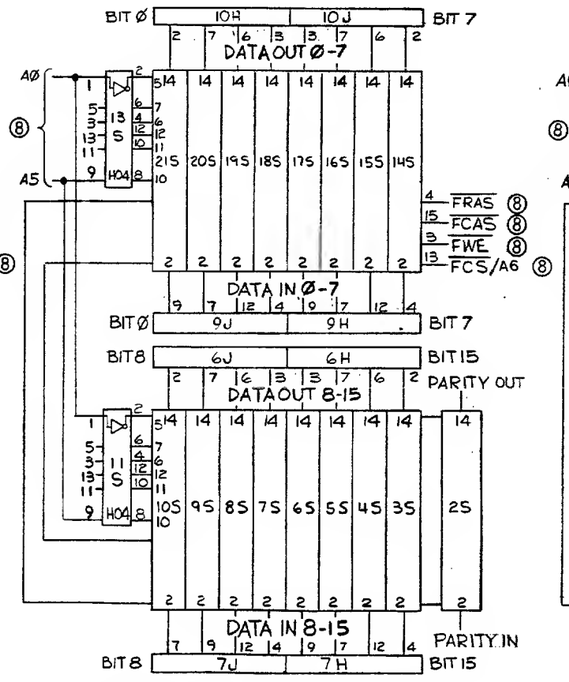
NOTE:
ALL PWR. PINS ON 4027-3 OR 4116-3 ARE:
+5V PIN 9
-5V PIN 1
GND PIN 16
+12V PIN 8

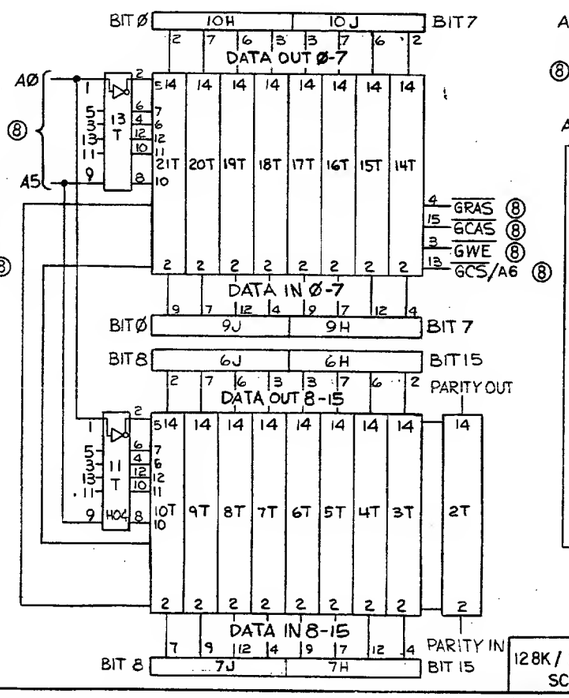


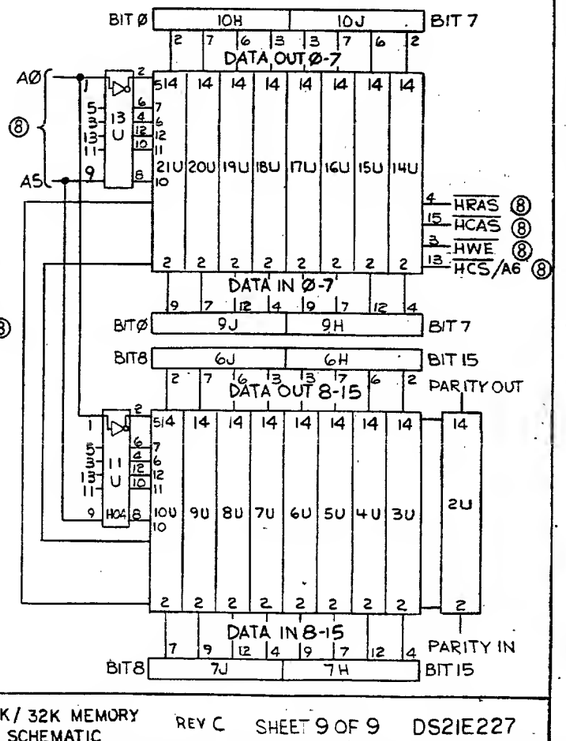




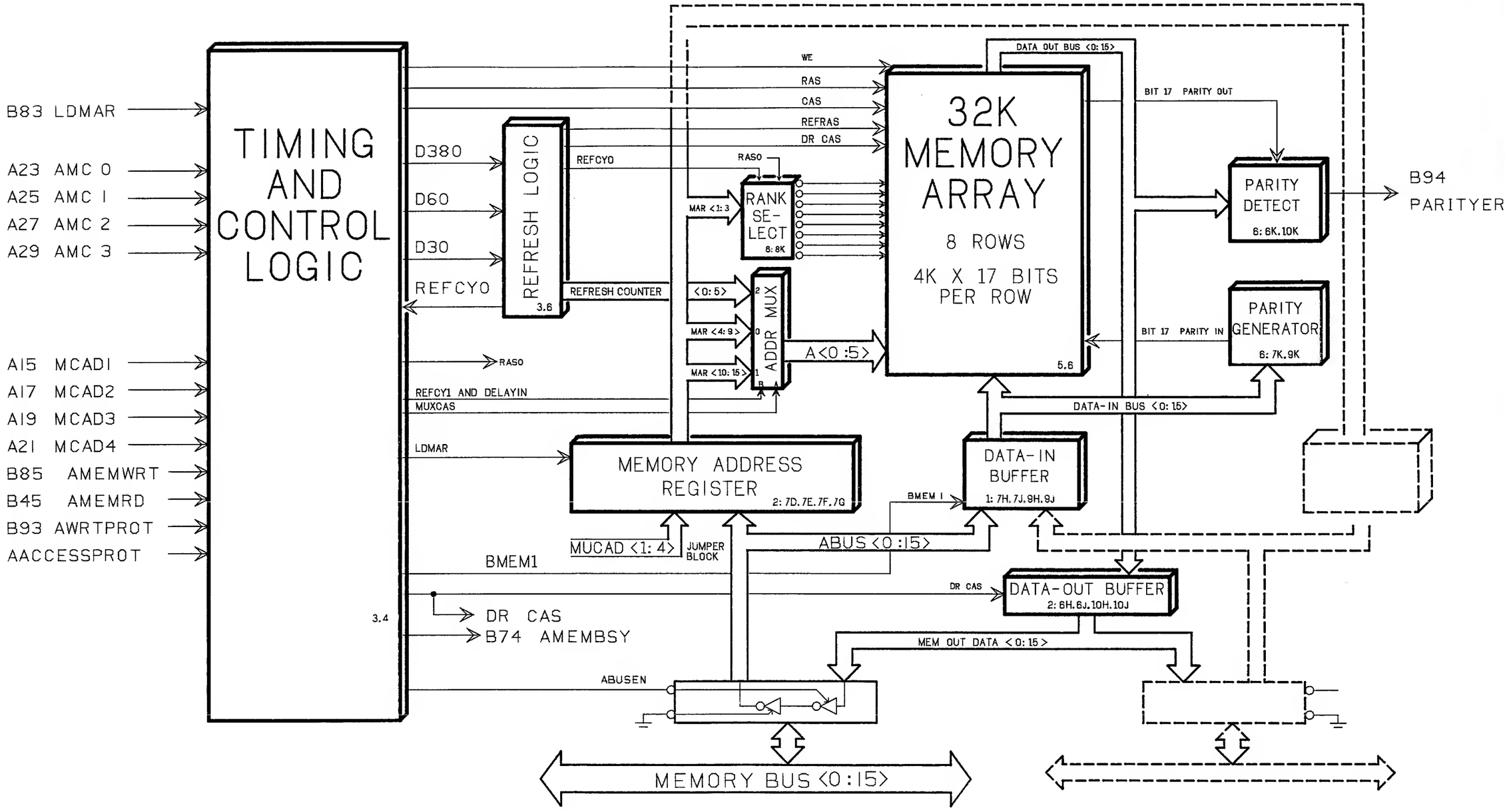








128K / 32K MEMORY SCHEMATIC REV C SHEET 9 OF 9 DS21E227

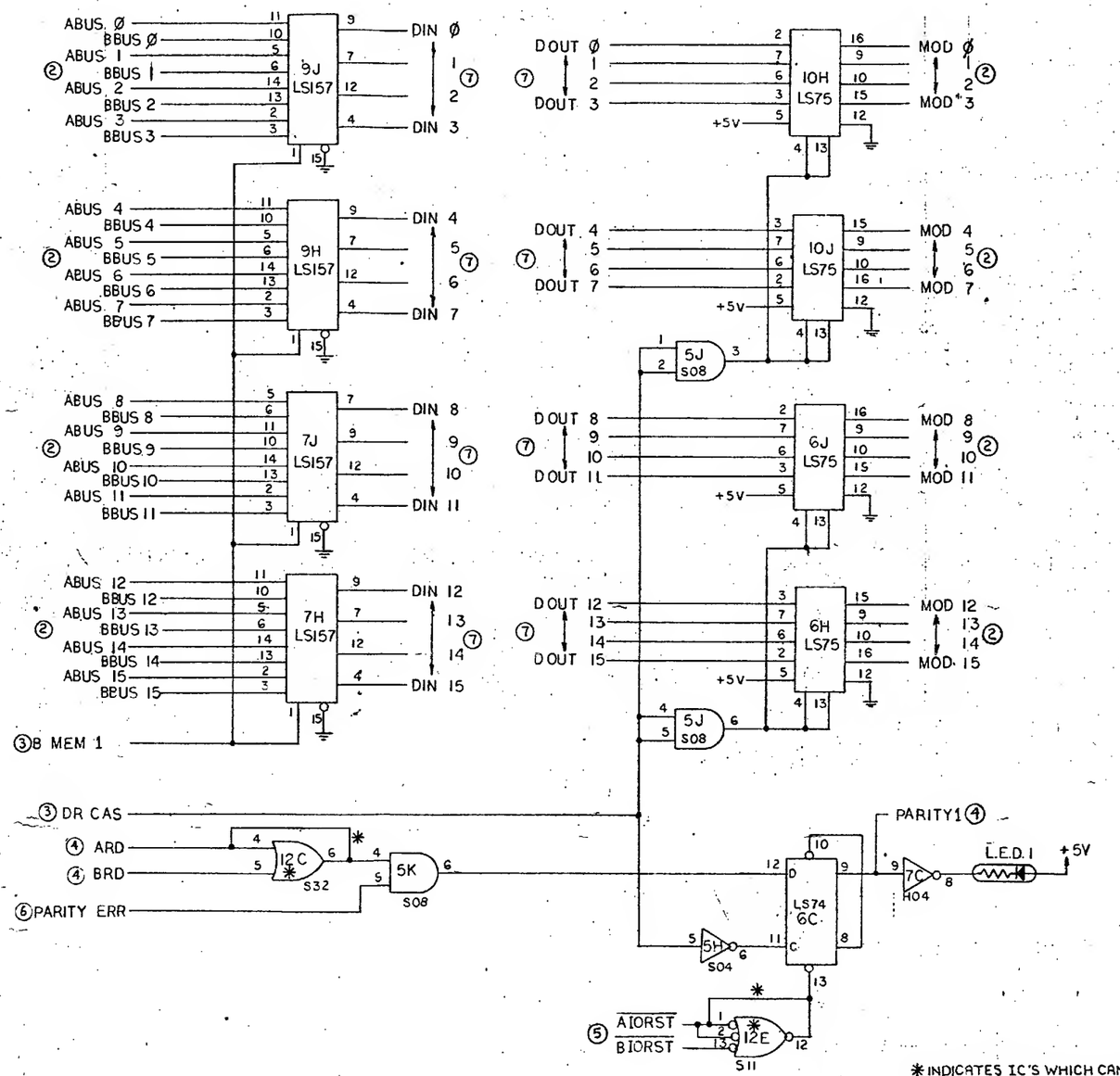


* ABUS <0,5:15> IF MAPPED; ABUS <0:15> IF UNMAPPED

DASHED LINES INDICATE B PORT

32K Memory Unit (Single Port)
DS21E102 (Obsolete)

	Sheet No.
Block Diagram	
Data Input/Output Logic	1
Bus and Memory Address Logic	2
Refresh Timing Logic	3
Bus Control Logic	4
I/O Logic	5
Typical Memory Rank	6
Parity Logic	6
Memory Array	7



B PORT CONNECTORS

CONN D

1	BINTPOUT	
11	BIORST	
	BCLR	
	BIOPLS	
	BINTA	
	BDS5	
21	BDS4	
	BDS3	
	BDS2	
	BDS1	
	BDSØ	
31	BRQENB	
	BDATA10	
	BDATA11	
	BDATA12	
41	BDATA13	
	BDATA14	
	BDATA15	
49	BINTR	50

CONN E

1	B MEM RD	
	B MEM WRT	
	BACCESS PROT	
	B WRT PROT	
	B MEM BUSY	
11	B MEM BUS 15	
	14	
	13	
	12	
	11	
21	1Ø	
	9	
	8	
	7	
	6	
31	5	
	4	
	3	
	2	
	1	
41	B MEM BUS Ø	
	BMC3	
	BMC2	
	BMC1	B PARITY ER
49	BMCØ	BLD MAR 50

ALL UNUSED PINS GRDED

VOLTAGE FEEDS FOR CONNECTORS PA, PB	
+12 VOLTS	B46, A7, A8
-5 VOLTS	B18
-12 VOLTS	B71, B72
+5 VOLTS	A/B3, A/B4, A/B97, A/B98
GND	A/B1, A/B2, A/B99, A/B100

DS21E102 D

SUPERSEDED BY DA21E250 ECO #3318 1/3/80 D. Stuart

DS21E102 Rev D 1977 [illegible]

DATA INPUT / OUTPUT LOGIC

* INDICATES IC'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY
	L21E009	1
	DA21E100	REF

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TOLERANCES: DECIMAL .XX = ± .01, .XXX = ± .005, .XXXX = ± .0010; FRACTIONAL = ± 1/64; ANGULAR = ± 1°00'

DRN T. Ribeiro 10/76; CHK [illegible] 1/76; ENGR [illegible] 1/76; PROJ [illegible] 2/78; MFG [illegible] 3/78

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	APPD	DATE
D	ECO # 2934	[illegible]	[illegible]
C/2	ECO # 2729	[illegible]	4/78
B/2	ECO # 2682	[illegible]	4/78
H/2	REL ECO # 2595	[illegible]	1/78

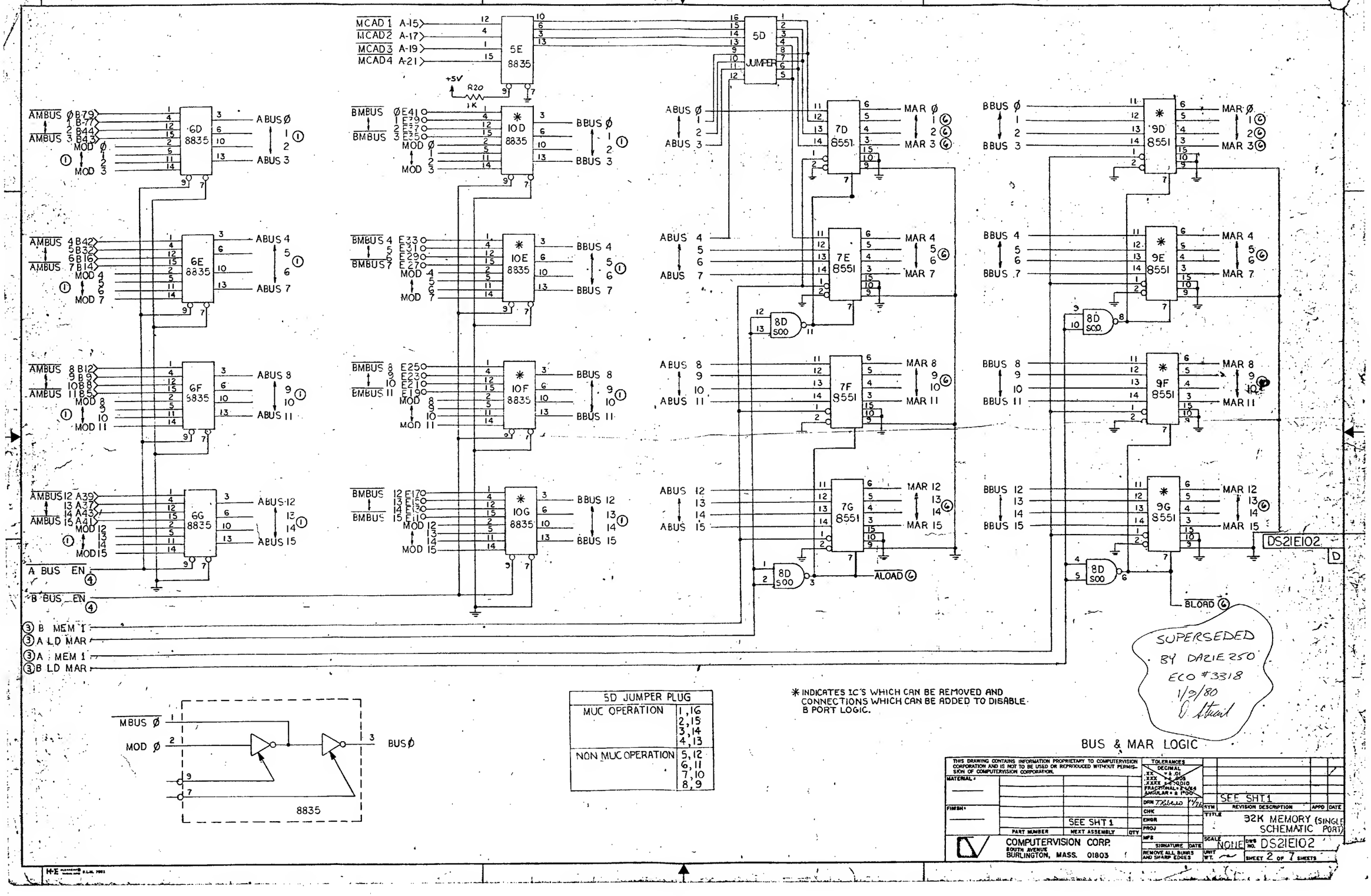
TITLE: 32K MEMORY (SINGLE PORT) SCHEMATIC

SCALE: NONE

DWG NO. DS21E102

UNIT WT. —

SHEET 1 OF 7 SHEETS



5D JUMPER PLUG	
MUC OPERATION	1,16 2,15 3,14 4,13
NON MUC OPERATION	5,12 6,11 7,10 8,9

* INDICATES IC'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.

SUPERSEDED BY DA21E250 ECO #3318 1/9/80 D. Attwell

BUS & MAR LOGIC

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TOLERANCES: DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010; FRACTIONAL ± 1/64; ANGULAR ± 1 DEG

MATERIAL

FINISH

DRN T.Kilard 1/9/80

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

PART NUMBER | NEXT ASSEMBLY | QTY

SEE SHT 1

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT 1		

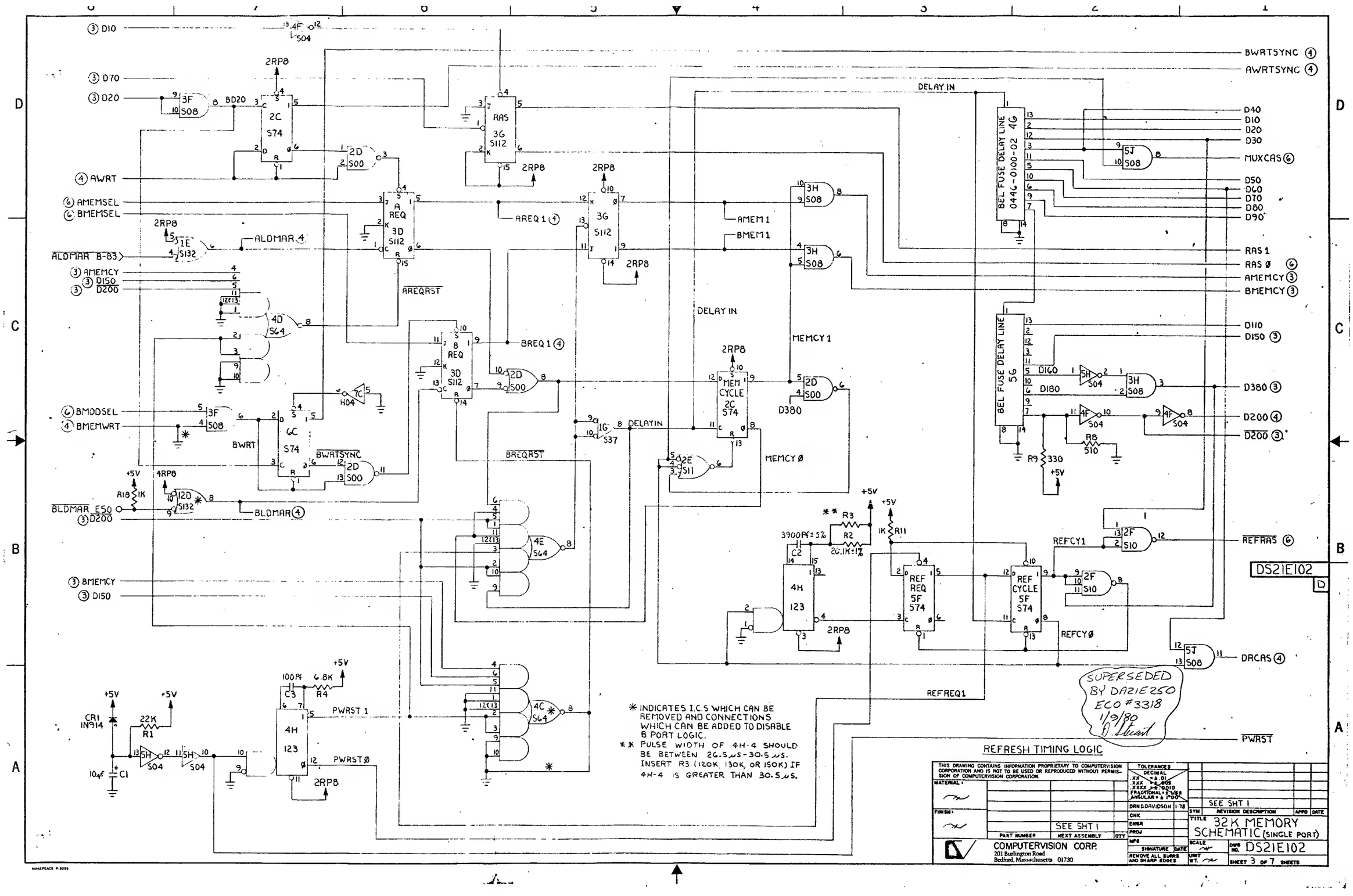
TITLE: 32K MEMORY (SINGLE PORT) SCHEMATIC

SCALE: NONE

DWG NO. DS21E102

UNIT WT.

SHEET 2 OF 7 SHEETS



* INDICATES I.C.S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.

** PULSE WIDTH OF 4H-4 SHOULD BE BETWEEN 26.5 μs - 30.5 μs. INSERT R3 (120K, 130K, OR 150K) IF 4H-4 IS GREATER THAN 30.5 μs.

REFRESH TIMING LOGIC

THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:

FINISH:

PART NUMBER	NEXT ASSEMBLY	QTY
	SEE SHT 1	

TOLERANCES DECIMAL .XX = ± .01 .XXX = ± .005 .XXXX = ± .0010 FRACTIONAL = ± 1/64 ANGULAR = ± 1°00'

DRN D.DAVIDSON 1-78

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHT 1		

TITLE 32K MEMORY SCHEMATIC (SINGLE PORT)

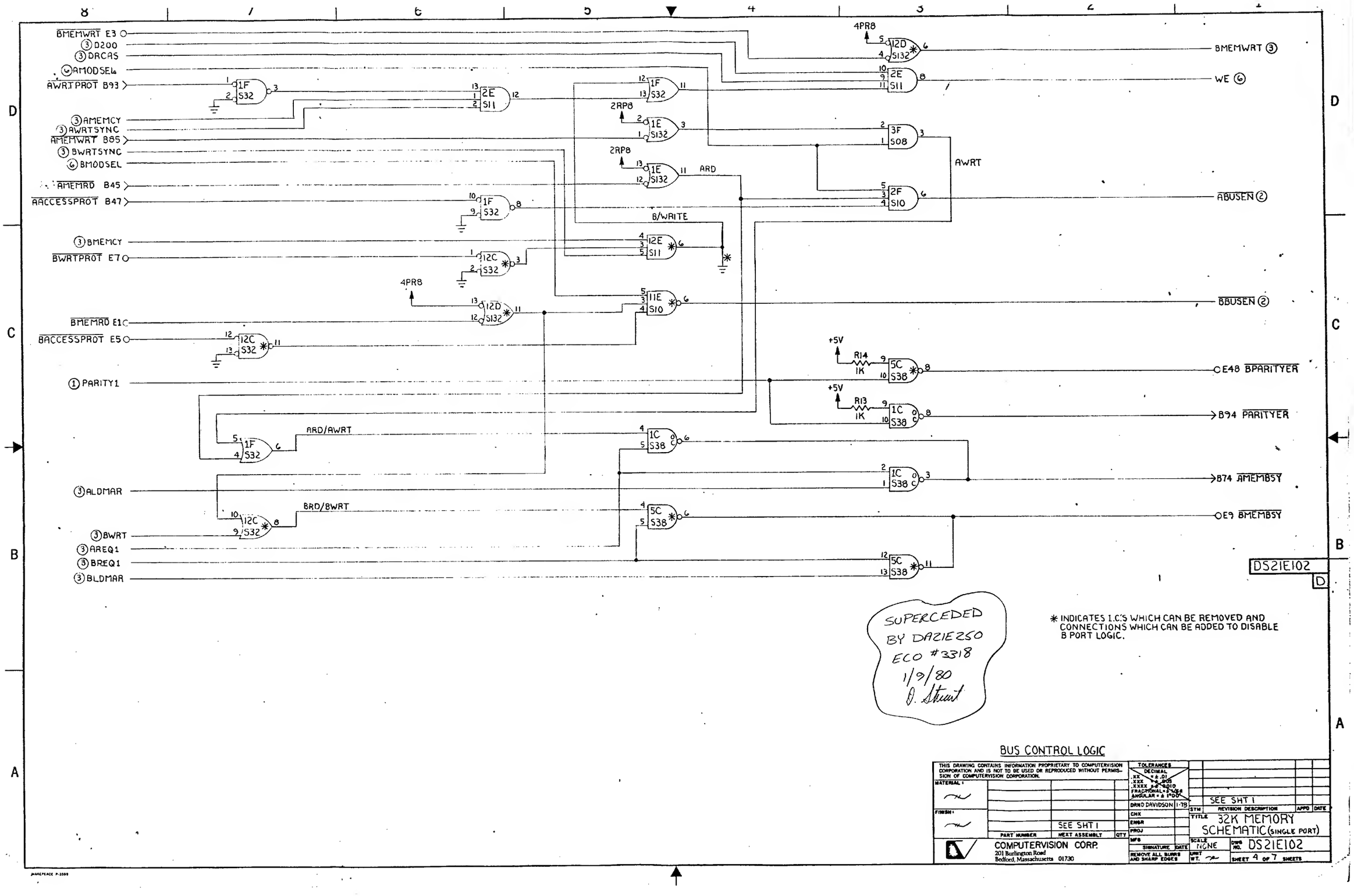
SCALE

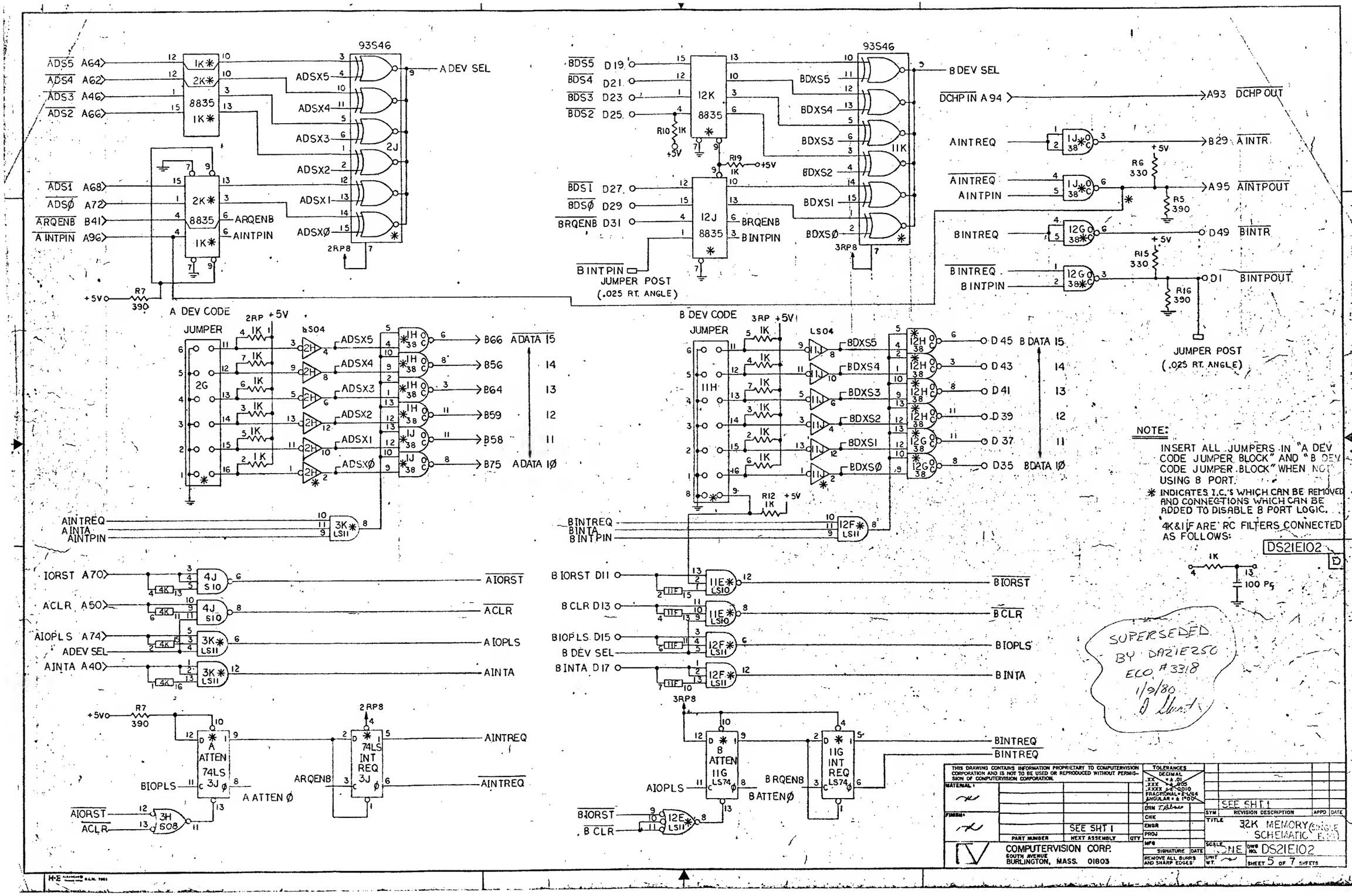
UNIT WT.

DWG NO. DS21E102

SHEET 3 OF 7 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730


BMEMWRT E3
(3) D200
(3) DRCAS
(6) AMODSEL4
AWRTPROT B93
(3) AMEMCY
(3) AWRTSYNC
AMEMWRT B85
(3) BWRTSYNC
(6) BMODSEL
AMEMRD B45
AACCESSPROT B47
(3) BMEMCY
BWRTPROT E7
BMEMRD E1
BACCESSPROT E5
(1) PARITY1
(3) ALDMAR
(3) BWRT
(3) AREQ1
(3) BREQ1
(3) BLDMAR
ARD/AWRT
BRD/BWRT
4PR8
2RP8
ARD
B/WRITE
AWRT
+5V
R14 1K
R13 1K
BMEMWRT (3)
WE (6)
ABUSEN (2)
BBUSEN (2)
E48 BPARITYER
B94 PARITYER
B74 AMEMBSY
E9 BMEMBSY
DS21E102
D
SUPERCEDED BY DAZIE250 ECO #3318 1/9/80 D. Stuart
* INDICATES I.C.'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.
BUS CONTROL LOGIC
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730
SEE SHT 1
DRND DAVIDSON 1-78
32K MEMORY SCHEMATIC (SINGLE PORT)
SCALE NONE
DWG NO. DS21E102
SHEET 4 OF 7 SHEETS



93S46
A DEV SEL
B DEV SEL
A DEV CODE JUMPER
B DEV CODE JUMPER
JUMPER POST (.025 RT. ANGLE)
NOTE:
INSERT ALL JUMPERS IN "A DEV CODE JUMPER BLOCK" AND "B DEV CODE JUMPER BLOCK" WHEN NOT USING B PORT.
* INDICATES I.C.'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.
4K&1F ARE RC FILTERS CONNECTED AS FOLLOWS:
DS21E102
SUPERSEDED BY DA21E250 ECO #3318 1/9/80
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
32K MEMORY SCHEMATIC
SEE SHT 1
DS21E102
SHEET 5 OF 7 SHEETS

DATA OUT Ø-7

DOUT Ø DOUT 1 DOUT 2 DOUT 3 DOUT 4 DOUT 5 DOUT 6 DOUT 7

DIN 0 DIN 1 DIN 2 DIN 3 DIN 4 DIN 5 DIN 6 DIN 7

DATA IN Ø-7 DATA OUT 8-15

DOUT 8 DOUT 9 DOUT 10 DOUT 11 DOUT 12 DOUT 13 DOUT 14 DOUT 15 PARITY OUT

DIN 8 DIN 9 DIN 10 DIN 11 DIN 12 DIN 13 DIN 14 DIN 15 PARITY IN

DATA IN 8-15

REFERENCE SHEET 1 FOR MEMORY DATA INPUT/OUTPUT INTERCONNECTIONS DEPICTS 1 OF 8 ROWS OF MEMORY. REMAINING 7 OF 8 ROWS ON SHEET 6.
MEMORY CHIPS MAY BE 4027P3 OR 4027N3.

SUPERSEDED BY DA21E250 ECO #3318 1/9/80 D. Stuart

MEM MODULE#	MC0	MC1	MC2	MC3	JUMPER POSITIONS
Ø	H	H	H	H	2,4,6,8
1	H	H	H	L	2,4,6,7
2	H	H	L	H	2,4,5,8
3	H	H	L	L	2,4,5,7
4	H	L	H	H	2,3,6,8
5	H	L	H	L	2,3,6,7
6	H	L	L	H	2,3,5,8
7	H	L	L	L	2,3,5,7
8	L	H	H	H	1,4,6,8
9	L	H	H	L	1,4,6,7
10	L	H	L	H	1,4,5,8
11	L	H	L	L	1,4,5,7
12	L	L	H	H	1,3,6,8
13	L	L	H	L	1,3,6,7
14	L	L	L	H	1,3,5,8
15	L	L	L	L	1,3,5,7

* INDICATES I.C.'S WHICH CAN BE REMOVED AND CONNECTIONS WHICH CAN BE ADDED TO DISABLE B PORT LOGIC.

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TOLERANCES DECIMAL .XX ± .01 .XXX ± .005 .XXXX ± .0010 FRACTIONAL ± 1/64 ANGULAR ± 5 DEG

SYM	REVISION DESCRIPTION	APPD	DATE
	SEE SHEET 1		

DRN S.R.T. 11/77
CHK 11/77
ENG 11/77
PROJ
MFG
SIGNATURE DATE

PART NUMBER SEE SHT 1 NEXT ASSEMBLY QTY

REMOVE ALL BURRS AND SHARP EDGES

SCALE NONE UNIT WT. NONE

TITLE 32K MEMORY (SINGLE PORT) SCHEMATIC

DWG NO. DS21E102

SHEET 6 OF 7 SHEETS

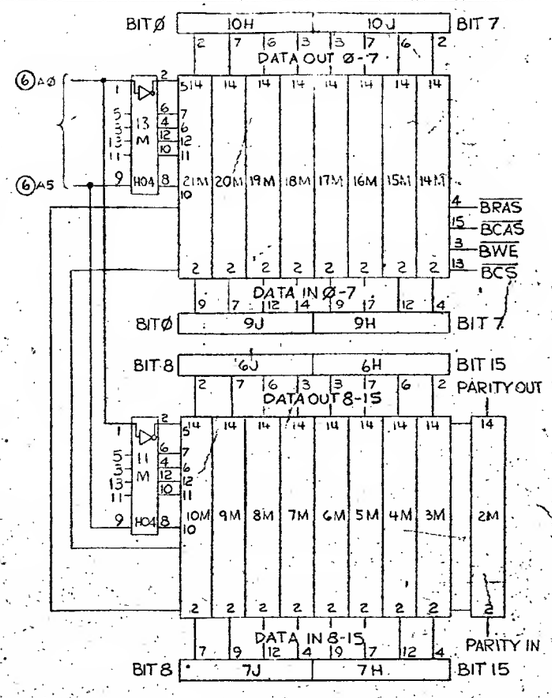
COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

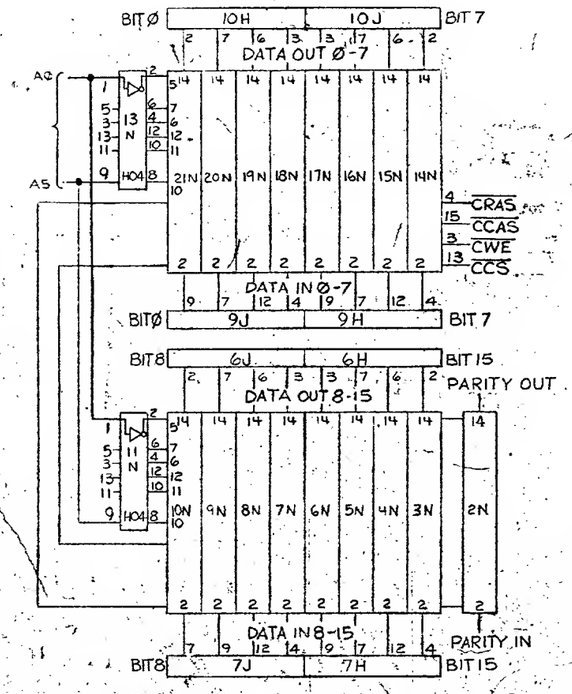
DS21E102 D

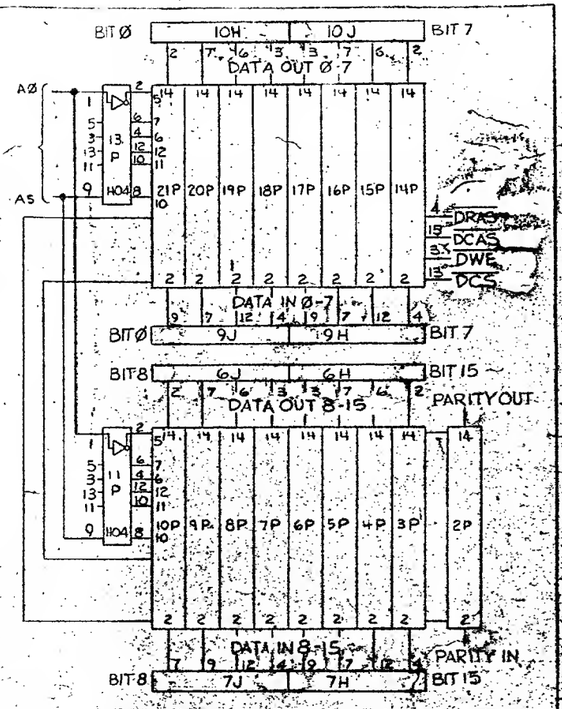
MEMORY ARRAY

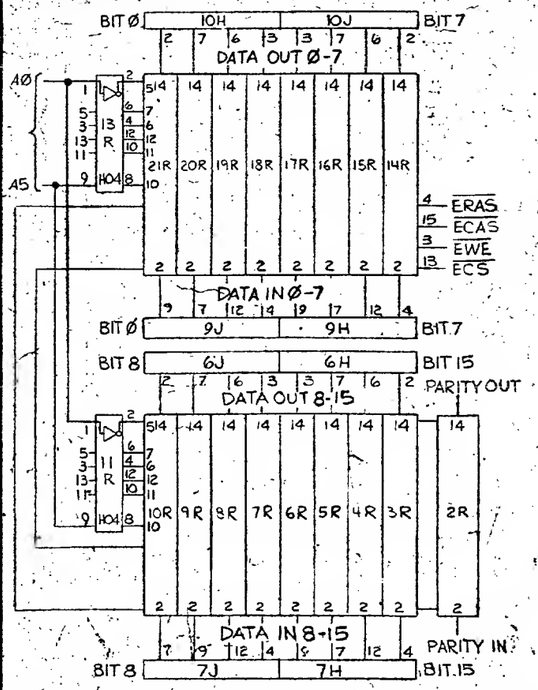
FOR MORE DETAIL OF TYPICAL 4K MEMORY SEE SHEET 5.
FOR MEMORY DATA INPUT/OUTPUT INTERCONNECTIONS, SEE SHEET 1.

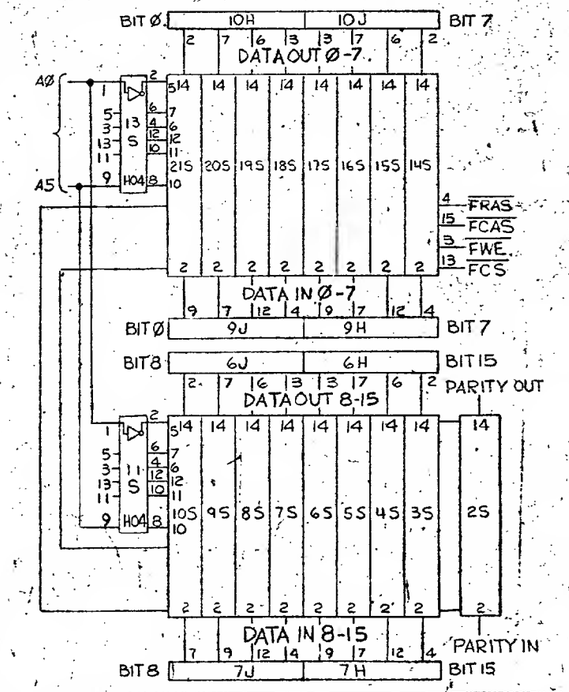
NOTE:
ALL PWR. PINS ON 4027-P3 OR N3 ARE:
+5V PIN 9
-5V PIN 1
GND PIN 16
+12V PIN 8

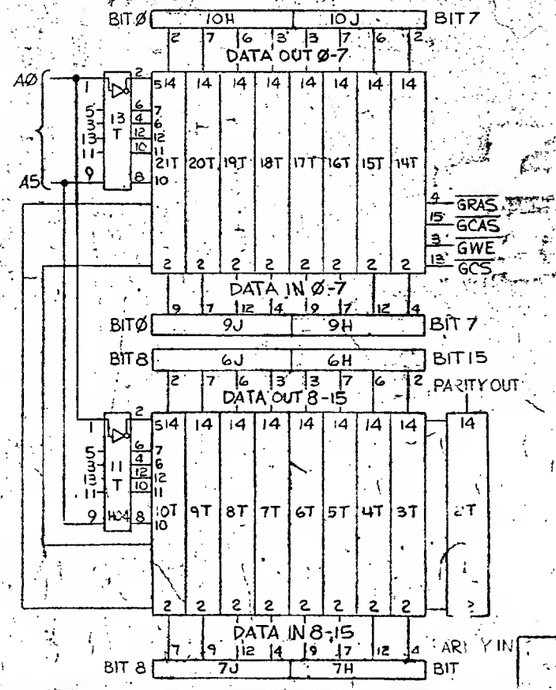


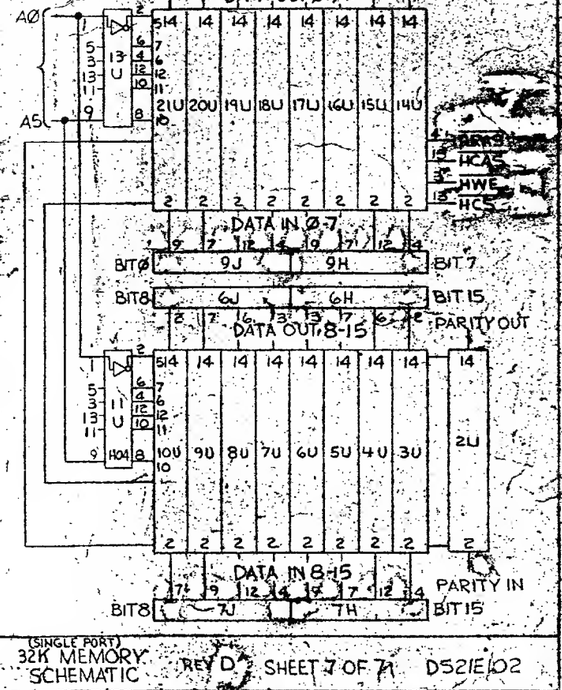












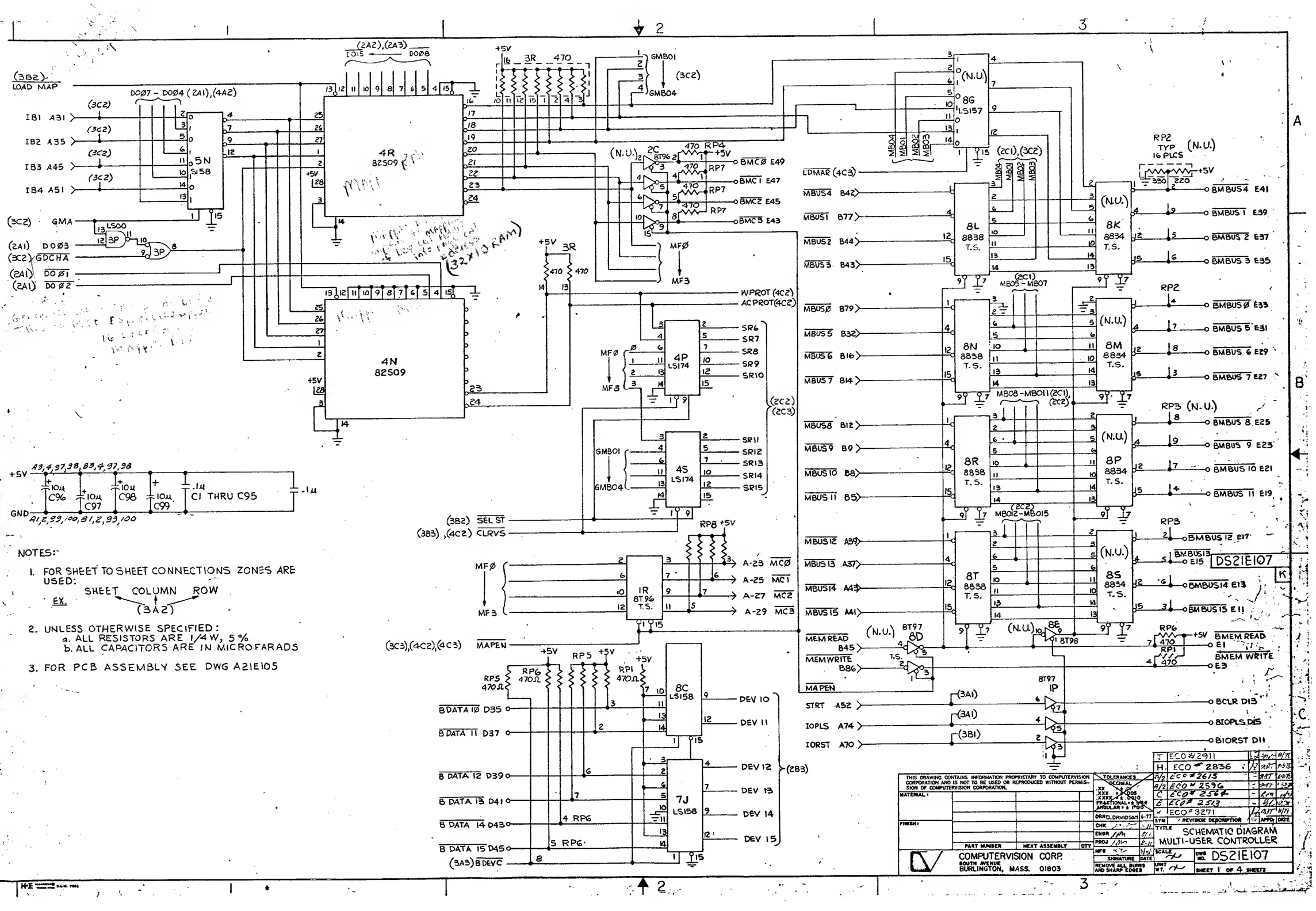
(SINGLE PORT)
32K MEMORY
SCHEMATIC

REV D SHEET 7 OF 7A D521E/02

Memory Management and Protection Unit

	Sheet No.
Block Diagram	
Mapper RAM	1
Bus Logic	1
Mapper Status	2
I/O Logic	3
Timing Logic	4
Protection Logic	4

ENABLE
STRT
CLR
IOPLS
DCHA
GDCHA
IOINST
DO 00
DATOA
DO 00
DATOB
INTER-FACE CONTROL LOGIC
3
STRT2
CLR2
IOPLS2
MAPEN
GMA
LOADMAP
SELST
ENPROT
DS <0:5>
DEVICE SELECT LOGIC
3: 1M.3L
USER
LDMAR
DONE
DATOC
LDIR
DATIA
DATIB
DATIC
DECODER
2: 6J
GS
INTPIN
RQENB
IORST
INTA
MSKO
SETDN
DOO
USER
INTER-RUPT LOGIC
3
INTPOUT
IORST
CLRVS
INTR
SELB
SELD
MAPDC
BIT 0 = GROUND
INVALID ADDRESS REGISTER
2: 7K.7M.7P.7S
INV<0:15>
INV<1:15>
GRD
INST. REGIS-TER
2
INST<0:15>
MEMORY BUS
<0:15>
TRANSCEIVER
MEMORY BUS <0:15>
DO <00:15>
LDMAR
0
1: 8G
1
IB<1:4>
DO 04:07
GMA
DO 03
A 0 1
1: 5N
MSB
GDCHA
RAM ADDRESS LINES
TRANSCEIVER
B PORT MEMORY BUS
MAPEN
LDMAP
RAM
1: 4N.4R
DO<01:02,08:15>
SEL ST
CLRVS
WPROT
ACPROT
STATUS REGIS-TER
1: 4P.4S
USEPRI (SR0)
WRVIOL (SR1)
SPVCALL (SR2)
ACCVIOL (SR3)
DCHVIOL (SR4)
DEFVIOL (SR5)
SR 6:7
SR 8:11
SR 12:15
MAPPER STATUS MULTIPLEXER
B
A
1
0
2
3
2: 6M 6N 6P 6R 6S 6T
DRIVERS AND RE-CEIVERS
2: 5K.5M.5P.5S
DO <00:15>
DO <00:15>
DATA BUS <0:15>
MUCAD 1
MUCAD 2
MUCAD 3
MUCAD 4
A 0
1
3: 3S
GMB <1:4>
MC0
MC1
MC2
MC3
1: 1R
MF<0:3>
2_8
IDENT. REGISTER
1: 7J.8C
DEV <10:15>
LINES 0:9 = GROUND
STRT2
CLR2
IOPLS2
IORST
CLRINT
LDMAR
LDIR
MAPEN
ENPROT
DEFER
DO<0,2,3,5,6>
TIMING AND CONTROL LOGIC
4
USER
SETDN
USERPI
WRTPROT
ACCESSPROT
PARITYER
MEMBUSY
GDCHA
SINGLECYCLE
SR <0:5>



NOTES:

1. FOR SHEET TO SHEET CONNECTIONS ZONES ARE USED:
   EX. SHEET COLUMN ROW (3A2)
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTORS ARE 1/4 W, 5%
   b. ALL CAPACITORS ARE IN MICROFARADS
3. FOR PCB ASSEMBLY SEE DWG A21E105

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SYM	REVISION DESCRIPTION	APPD	DATE
J	ECO # 2911		11/78
H	ECO # 2836		4-5-78
B/2	ECO # 2615		6-2-78
A/2	ECO # 2596		1-23-78
C	ECO # 2564		11/78
E	ECO # 2513		10/78
K	ECO # 3271		11/79

TOLERANCES: DECIMAL .XX ± .01, .XXX ± .005, .XXXX ± .0010; FRACTIONAL ± 1/64; ANGULAR ± 1°00'

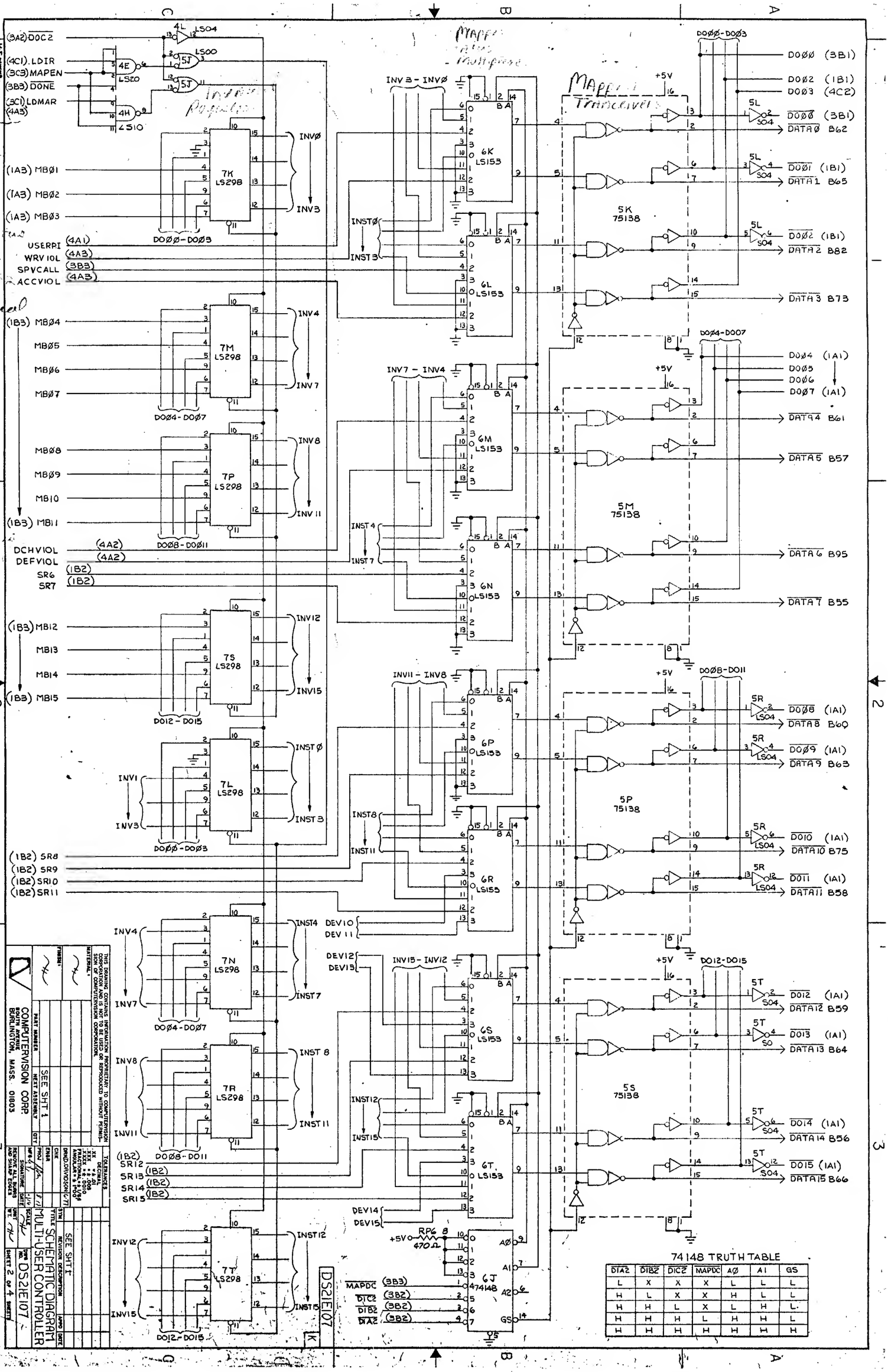
DRN D. DAVIDSON 6-77
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

MATERIAL:
FINISH:
PART NUMBER | NEXT ASSEMBLY | QTY

COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803

TITLE: SCHEMATIC DIAGRAM MULTI-USER CONTROLLER

SCALE
DWG NO. DS21E107
UNIT WT.
SHEET 1 OF 4 SHEETS


(3A2) DOC2
(4C1) LDIR
(3C3) MAPEN
(3B3) DONE
(3C) LDMAR
(4A3)
4L LS04
4E LS20
5J LS00
5J
4H LS10
7K LS298
INVØ
INV3
DOØØ-DOØ3
(1A3) MBØ1
(1A3) MBØ2
(1A3) MBØ3
USERPI (4A1)
WRVIOL (4A3)
SPVCALL (3B3)
ACCVIOL (4A3)
INV3 - INVØ
6K LS153
6L LS153
INSTØ
INST3
5K 75138
DOØØ-DOØ3
DOØØ (3B1)
DOØ2 (1B1)
DOØ3 (4C2)
DOØØ (3B1)
DATAØ B62
DOØ1 (1B1)
DATA1 B65
DOØ2 (1B1)
DATA2 B82
DATA3 B73
+5V
5L SO4
7M LS298
INV4
INV7
DOØ4-DOØ7
(1B3) MBØ4
MBØ5
MBØ6
MBØ7
INV7 - INV4
6M LS153
6N LS153
INST4
INST7
5M 75138
DOØ4-DOØ7
DOØ4 (1A1)
DOØ5
DOØ6
DOØ7 (1A1)
DATA4 B61
DATA5 B57
DATA6 B95
DATA7 B55
7P LS298
INV8
INV11
DOØ8-DOØ11
MBØ8
MBØ9
MB10
(1B3) MB11
DCHVIOL (4A2)
DEFVIOL (4A2)
SR6 (1B2)
SR7 (1B2)
7S LS298
INV12
INV15
DO12-DO15
(1B3) MB12
MB13
MB14
(1B3) MB15
INV11 - INV8
6P LS153
6R LS153
INST8
INST11
5P 75138
DOØ8-DO11
DOØ8 (1A1)
DOØ9 (1A1)
DO10 (1A1)
DO11 (1A1)
DATA8 B60
DATA9 B63
DATA10 B75
DATA11 B58
5R LS04
7L LS298
INV1
INV3
DOØØ-DOØ3
INSTØ
INST3
(1B2) SR8
(1B2) SR9
(1B2) SR10
(1B2) SR11
7N LS298
INV4
INV7
DOØ4-DOØ7
INST4
INST7
DEV10
DEV11
DEV12
DEV13
INV15 - INV12
6S LS153
6T LS153
INST12
INST15
5S 75138
DO12-DO15
DO12 (1A1)
DO13 (1A1)
DO14 (1A1)
DO15 (1A1)
DATA12 B59
DATA13 B64
DATA14 B56
DATA15 B66
5T SO
7R LS298
INV8
INV11
DOØ8-DO11
INST8
INST11
(1B2) SR12
(1B2) SR13
(1B2) SR14
(1B2) SR15
DEV14
DEV15
RP6 8
470Ω
+5V
6J 74148
A0
A1
A2
GS
MAPDC (3B3)
DIC2 (3B2)
DIB2 (3B2)
DIA2 (3B2)
7T LS298
INV12
INV15
DO12-DO15
INST12
INST15
DS2IE107
K
74148 TRUTH TABLE
DIA2 DIB2 DIC2 MAPDC A0 A1 GS
L X X X L L L
H L X X H L L
H H L X L H L
H H H L H H L
H H H H H H H
COMPUTERVISION CORP.
BURLINGTON, MASS. 01803
SEE SHT 1
MULTI-USER CONTROLLER
SCHEMATIC DIAGRAM
DS2IE107
SHEET 2 OF 4 SHEETS
SEE SHT 1
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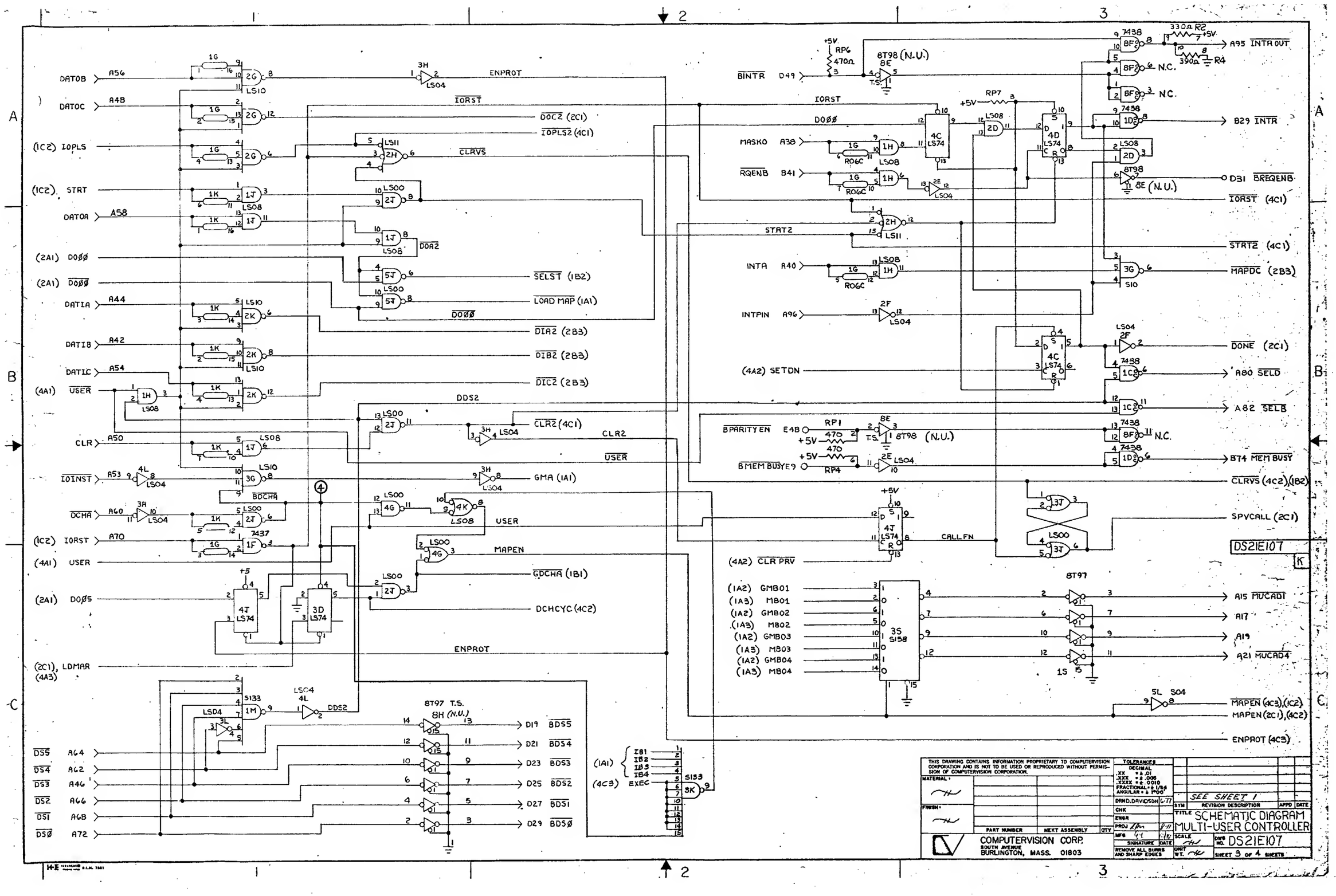
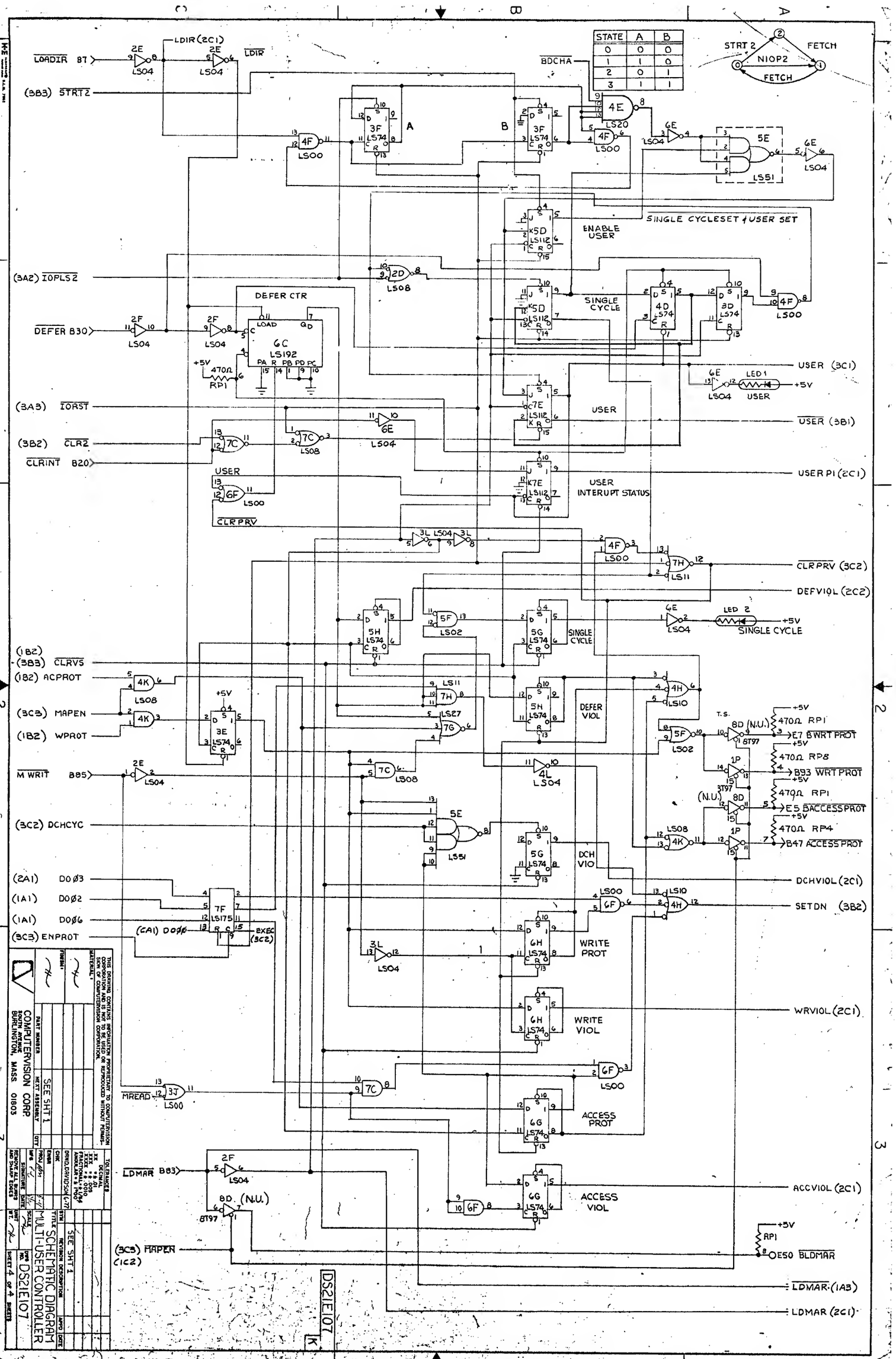
MATERIAL
FINISH
PART NUMBER
NEXT ASSEMBLY
USED
ENGR
CHK
PROJ
MFG
SIGNATURE
DATE
SCALE
SIZE
DWG NO
REVISION DESCRIPTION
APPD
DATE
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONAL
XX ± 0.03
XXX ± 0.010
ANGULAR ± 1°
DRWD DRVDSON 6/77
DO NOT SCALE PRINT
REVISIONS ARE LISTED ON SHEET 1

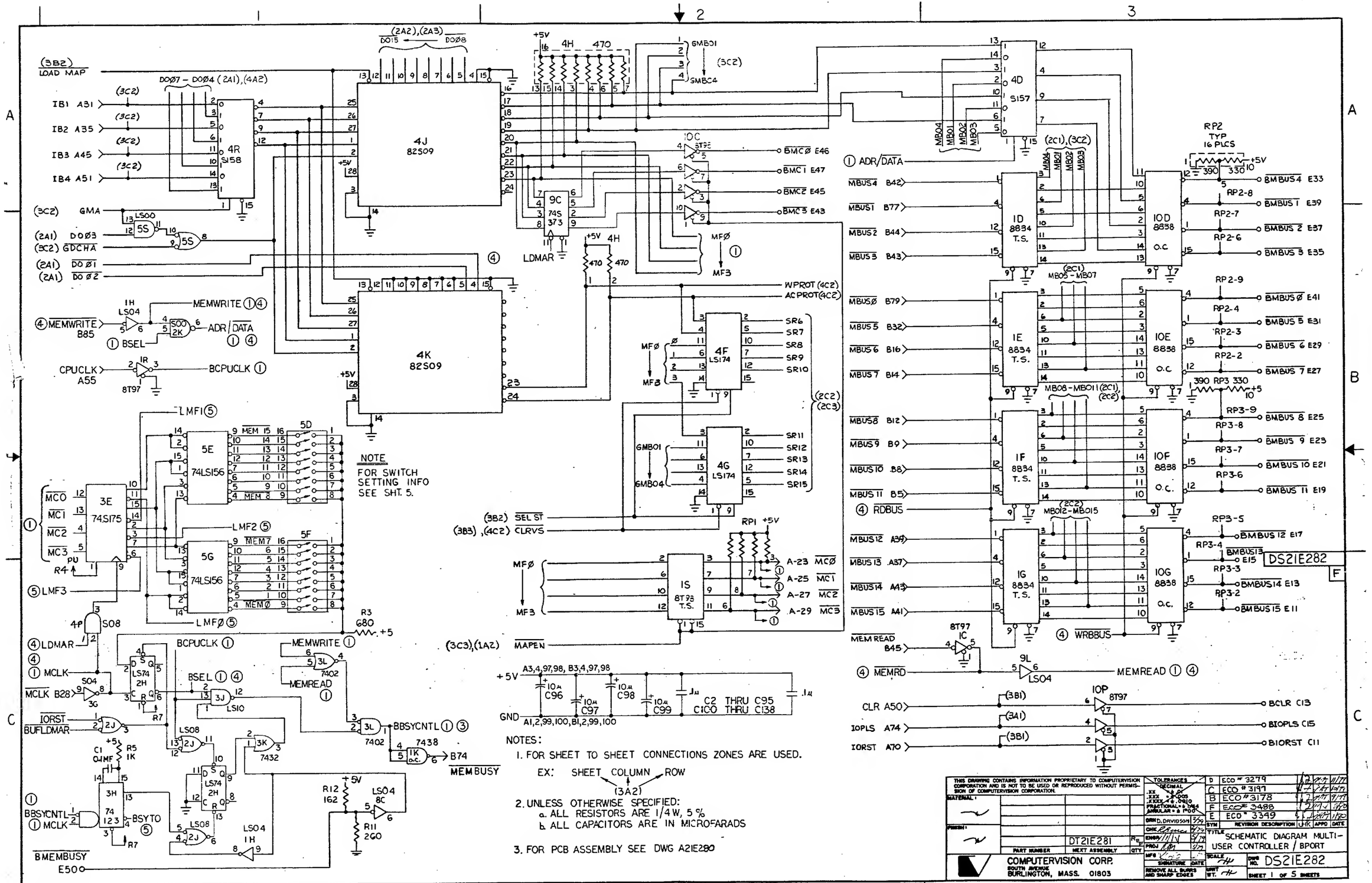

DATOB A56
DATOC A4B
(1C2) IOPLS
(1C2) STRT
DATOA A58
(2A1) DOØØ
(2A1) DOØØ
DATIA A44
DATIB A42
DATIC A54
(4A1) USER
CLR A50
IOINST A53
DCHA A60
(1C2) IORST A70
(4A1) USER
(2A1) DOØ5
(2C1), LDMAR (4A3)
ENPROT
IORST
DOC2 (2C1)
IOPLS2 (4C1)
CLRVS
DOA2
SELST (1B2)
LOAD MAP (1A1)
DOØØ
DIA2 (2B3)
DIB2 (2B3)
DIC2 (2B3)
DDS2
CLR2 (4C1)
CLR2
USER
GMA (1A1)
BDCHA
USER
MAPEN
GDCHA (1B1)
DCHCYC (4C2)
ENPROT
DS5 A64
DS4 A62
DS3 A46
DS2 A66
DS1 A6B
DSØ A72
D19 BDS5
D21 BDS4
D23 BDS3
D25 BDS2
D27 BDS1
D29 BDSØ
(1A1) IB1 IB2 IB3 IB4
(4C3) EXEC
BINTR D49
IORST
DOØØ
MASKO A38
RQENB B41
STRT2
INTA A40
INTPIN A96
(4A2) SETDN
BPARITYEN E4B
BMEMBUSYE9
(4A2) CLR PRV
(1A2) GMB01
(1A3) MB01
(1A2) GMB02
(1A3) MB02
(1A2) GMB03
(1A3) MB03
(1A2) GMB04
(1A3) MB04
CALLFN
A95 INTR OUT
N.C.
N.C.
B29 INTR
D31 BREQENB
IORST (4C1)
STRT2 (4C1)
MAPDC (2B3)
DONE (2C1)
A80 SELD
A82 SELB
N.C.
B74 MEM BUSY
CLRVS (4C2),(1B2)
SPVCALL (2C1)
DS21E107
K
A15 MUCAD1
A17
A19
A21 MUCAD4
MAPEN (4C3),(1C2)
MAPEN (2C1),(4C2)
ENPROT (4C3)
SEE SHEET 1
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
TITLE SCHEMATIC DIAGRAM
MULTI-USER CONTROLLER
DWG NO. DS21E107
SHEET 3 OF 4 SHEETS



STATE A B
0 0 0
1 1 0
2 0 1
3 1 1
STRT 2
FETCH
N1OP2
FETCH
LOADIR B7
LDIR (2C1)
LDIR
(3B3) STRT2
BDCHA
ENABLE USER
SINGLE CYCLESET & USER SET
(3A2) IOPLS2
DEFER CTR
DEFER B30
SINGLE CYCLE
USER (3C1)
USER
USER (3B1)
(3A3) IORST
(3B2) CLR2
CLRINT B20
USER INTERUPT STATUS
USER P1 (2C1)
CLRPRV
CLRPRV (3C2)
DEFVIOL (2C2)
SINGLE CYCLE
(1B2)
(3B3) CLRVS
(1B2) ACPROT
(3C3) MAPEN
(1B2) WPROT
DEFER VIOL
M WRIT B85
(3C2) DCHCYC
DCH VIO
DCHVIOL (2C1)
(2A1) DOØ3
(1A1) DOØ2
(1A1) DOØ6
(3C3) ENPROT
(CA1) DOØØ
EXEC (3C2)
SETDN (3B2)
WRITE PROT
WRITE VIOL
WRVIOL (2C1)
MREAD
ACCESS PROT
LDMAR B83
ACCESS VIOL
ACCVIOL (2C1)
(3C3) MAPEN (1C2)
BLDMAR
LDMAR (1A3)
LDMAR (2C1)
470Ω RP1
E7 BWRT PROT
470Ω RP8
B93 WRT PROT
470Ω RP1
E5 BACCESS PROT
470Ω RP4
B47 ACCESS PROT
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
SEE SHT 1
SCHEMATIC DIAGRAM
MULTI-USER CONTROLLER
DS21E107
SHEET 4 OF 4 SHEETS

B-Port Memory Management and Protection Unit

	Sheet No.
Mapper RAM	1
Bus Logic	1
Mapper Status Logic	2
I/O Logic	3
Timing Logic	4
Protection Logic	4
Switch Settings	5
Jumper Configuration	5
B-Port Connector Pinouts	5



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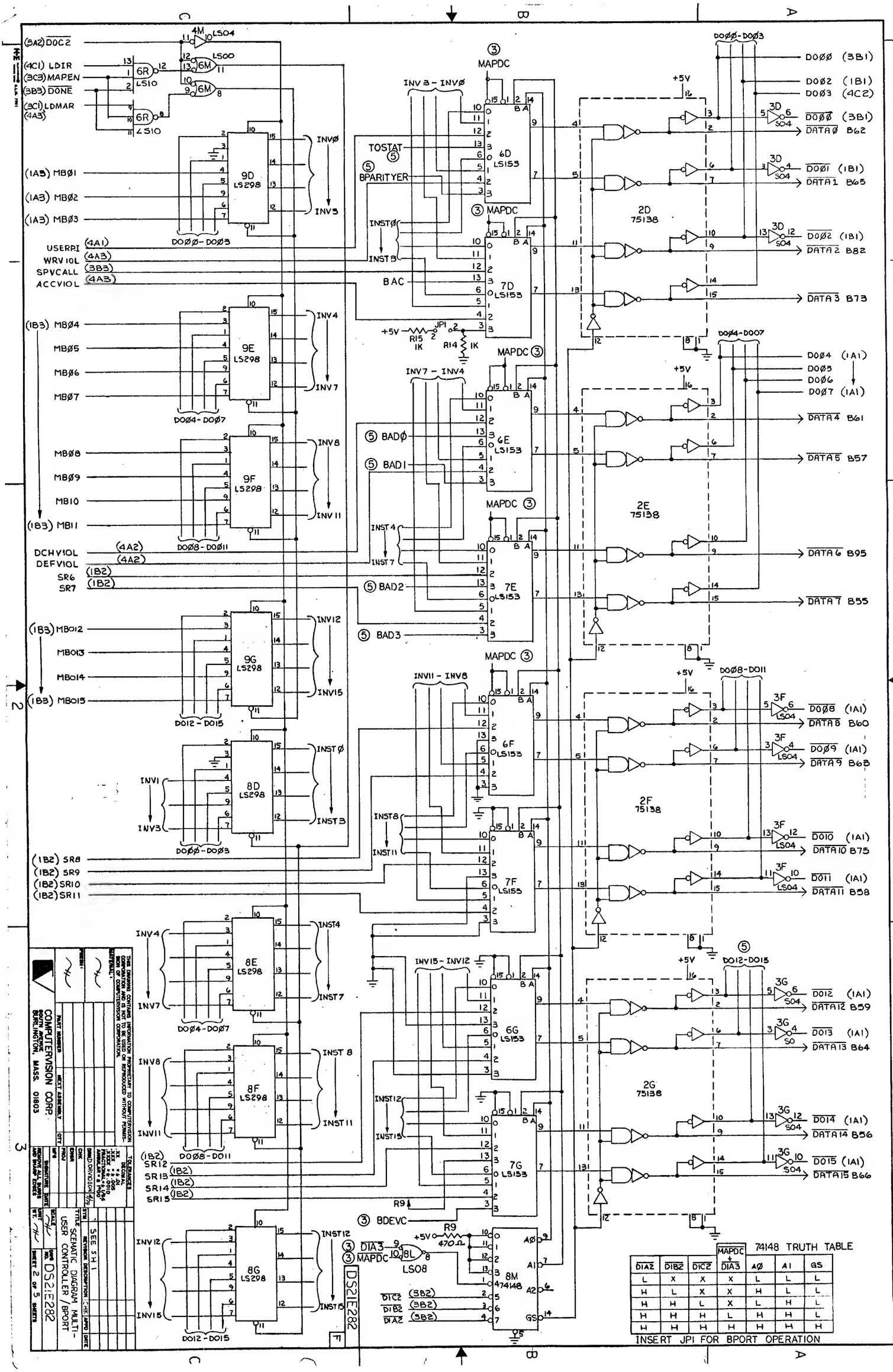
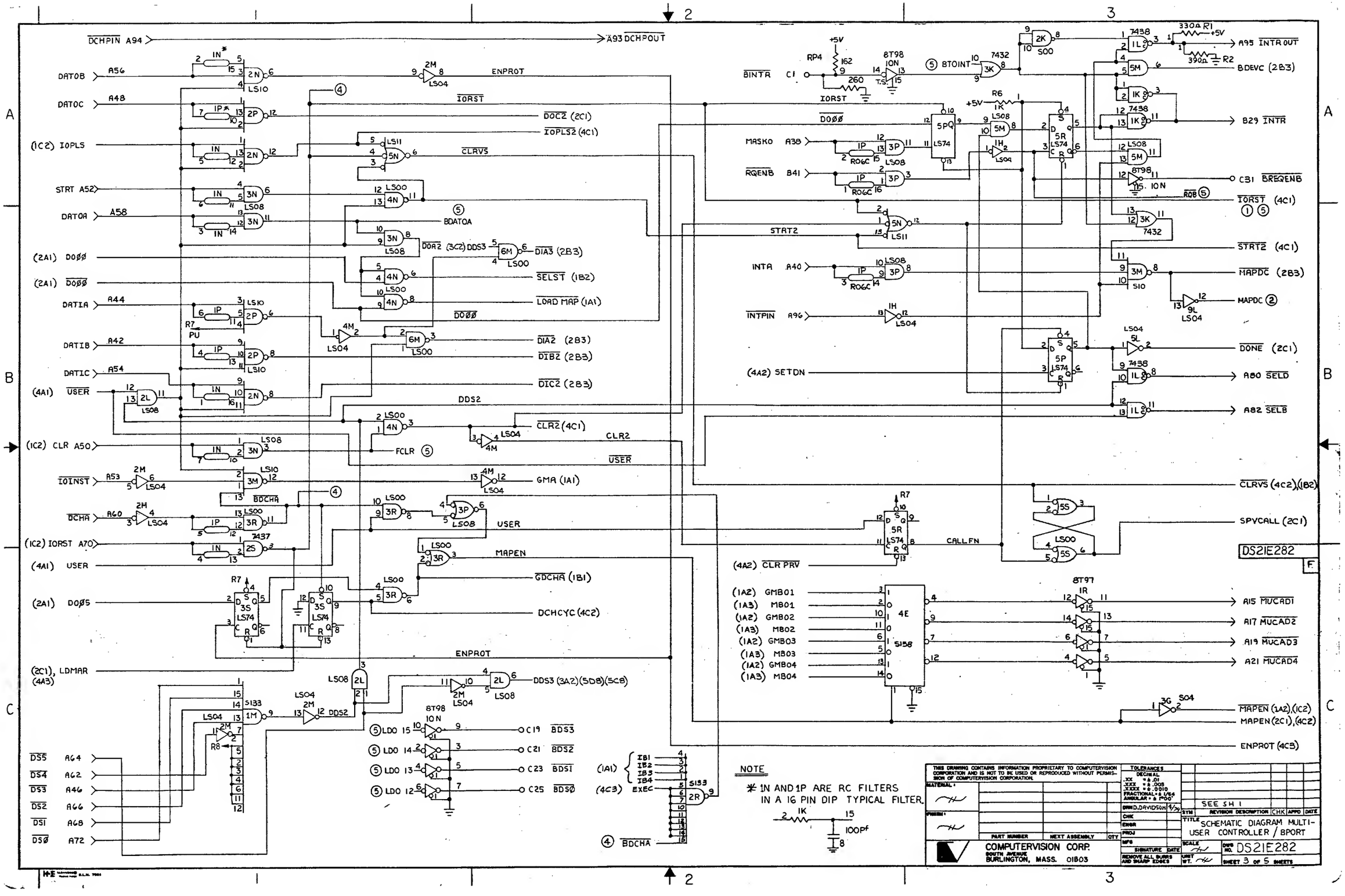

(3A2) DOC2
(4C1) LDIR
(3C3) MAPEN
(3B3) DONE
(3C1) LDMAR
(4A3)
4M LS04
LS00
LS10
LS10
6R
6M
9D LS298
9E LS298
9F LS298
9G LS298
8D LS298
8E LS298
8F LS298
8G LS298
INVØ
INV3
INV4
INV7
INV8
INV11
INV12
INV15
INST Ø
INST3
INST4
INST7
INST 8
INST11
INST12
INST15
MB Ø1
MB Ø2
MB Ø3
MB Ø4
MB Ø5
MB Ø6
MB Ø7
MB Ø8
MB Ø9
MB10
MB11
MB012
MB013
MB014
MB015
DØØ-DØ3
DØ4-DØ7
DØ8-DØ11
D12-D15
USERRI (4A1)
WRV10L (4A3)
SPVCALL (3B3)
ACCV10L (4A3)
DCHV10L (4A2)
DEFV10L (4A2)
SR6 (1B2)
SR7 (1B2)
SR8 (1B2)
SR9 (1B2)
SR10 (1B2)
SR11 (1B2)
SR12 (1B2)
SR13 (1B2)
SR14 (1B2)
SR15 (1B2)
③ MAPDC
INV3 - INVØ
6D LS153
TOSTAT ⑤
⑤ BPARITYER
INSTØ
INST3
BAC
7D LS153
+5V
JP1
R15 1K
R14 1K
INV7 - INV4
6E LS153
⑤ BADØ
⑤ BAD1
INST4
INST7
7E LS153
⑤ BAD2
⑤ BAD3
INV11 - INV8
6F LS153
INST8
INST11
7F LS153
INV15 - INV12
6G LS153
INST12
INST15
7G LS153
R9
③ BDEVC
R9 470Ω
③ DIA3
③ MAPDC
10L LS08
8M 74148
DIC2 (3B2)
DIB2 (3B2)
DIA2 (3B2)
DØØ-DØ3
DØ4-DØ07
DØ8-DØ11
⑤ D12-D15
DØØ (3B1)
DØ2 (1B1)
DØ3 (4C2)
DØØØ (3B1)
DATAØ B62
DØØ1 (1B1)
DATA1 B65
DØØ2 (1B1)
DATA2 B82
DATA3 B73
2D 75138
DØ4 (1A1)
DØ5
DØ6
DØ7 (1A1)
DATA4 B61
DATA5 B57
2E 75138
DATA6 B95
DATA7 B55
DØ08 (1A1)
DATA8 B60
DØ09 (1A1)
DATA9 B68
2F 75138
DØ10 (1A1)
DATA10 B75
DØ11 (1A1)
DATA11 B58
DØ12 (1A1)
DATA12 B59
DØ13 (1A1)
DATA13 B64
2G 75138
DØ14 (1A1)
DATA14 B56
DØ15 (1A1)
DATA15 B66
3D S04
3F LS04
3G S04
74148 TRUTH TABLE
MAPDC + DIA3
DIA2 DIB2 DIC2 A0 A1 GS
INSERT JPI FOR BPORT OPERATION
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
TITLE SCEMATIC DIAGRAM MULTI-USER CONTROLLER/BPORT
SIZE DWG NO DS21E282
SHEET 2 OF 5 SHEETS
SEE SH 1
DS21E282



DCHPIN A94
A93 DCHPOUT
DATOB A56
DATOC A48
(1C2) IOPLS
STRT A52
DATOA A58
(2A1) DOØØ
(2A1) DOØØ
DATIA A44
DATIB A42
DATIC A54
(4A1) USER
(1C2) CLR A50
IOINST A53
DCHA A60
(1C2) IORST A70
(4A1) USER
(2A1) DOØ5
(2C1), LDMAR (4A3)
DS5 A64
DS4 A62
DS3 A46
DS2 A66
DS1 A68
DSØ A72
ENPROT
IORST
DOC2 (2C1)
IOPLS2 (4C1)
CLRVS
BDATOA
DOA2 (3C2) DDS3
DIA3 (2B3)
SELST (1B2)
LOAD MAP (1A1)
DOØØ
DIA2 (2B3)
DIB2 (2B3)
DIC2 (2B3)
DDS2
CLR2 (4C1)
CLR2
FCLR
USER
GMA (1A1)
BDCHA
USER
MAPEN
GDCHA (1B1)
DCHCYC (4C2)
ENPROT
DDS3 (3A2)(5D8)(5C8)
DDS2
LDO 15
LDO 14
LDO 13
LDO 12
C19 BDS3
C21 BDS2
C23 BDS1
C25 BDSØ
(1A1) IB1 IB2 IB3 IB4
(4C3) EXEC
BDCHA
BINTR C1
IORST
DOØØ
MASKO A38
RQENB B41
STRT2
INTA A40
INTPIN A96
(4A2) SETDN
CALLFN
(4A2) CLR PRV
(1A2) GMB01
(1A3) MB01
(1A2) GMB02
(1A3) MB02
(1A2) GMB03
(1A3) MB03
(1A2) GMB04
(1A3) MB04
BTOINT
A95 INTR OUT
BDEVC (2B3)
B29 INTR
C31 BREQENB
RQB
IORST (4C1)
STRT2 (4C1)
MAPDC (2B3)
MAPDC
DONE (2C1)
A80 SELD
A82 SELB
CLRVS (4C2),(1B2)
SPVCALL (2C1)
DS21E282
A15 MUCAD1
A17 MUCAD2
A19 MUCAD3
A21 MUCAD4
MAPEN (1A2),(1C2)
MAPEN (2C1),(4C2)
ENPROT (4C3)
NOTE
* 1N AND 1P ARE RC FILTERS IN A 16 PIN DIP TYPICAL FILTER.
1K
100pF
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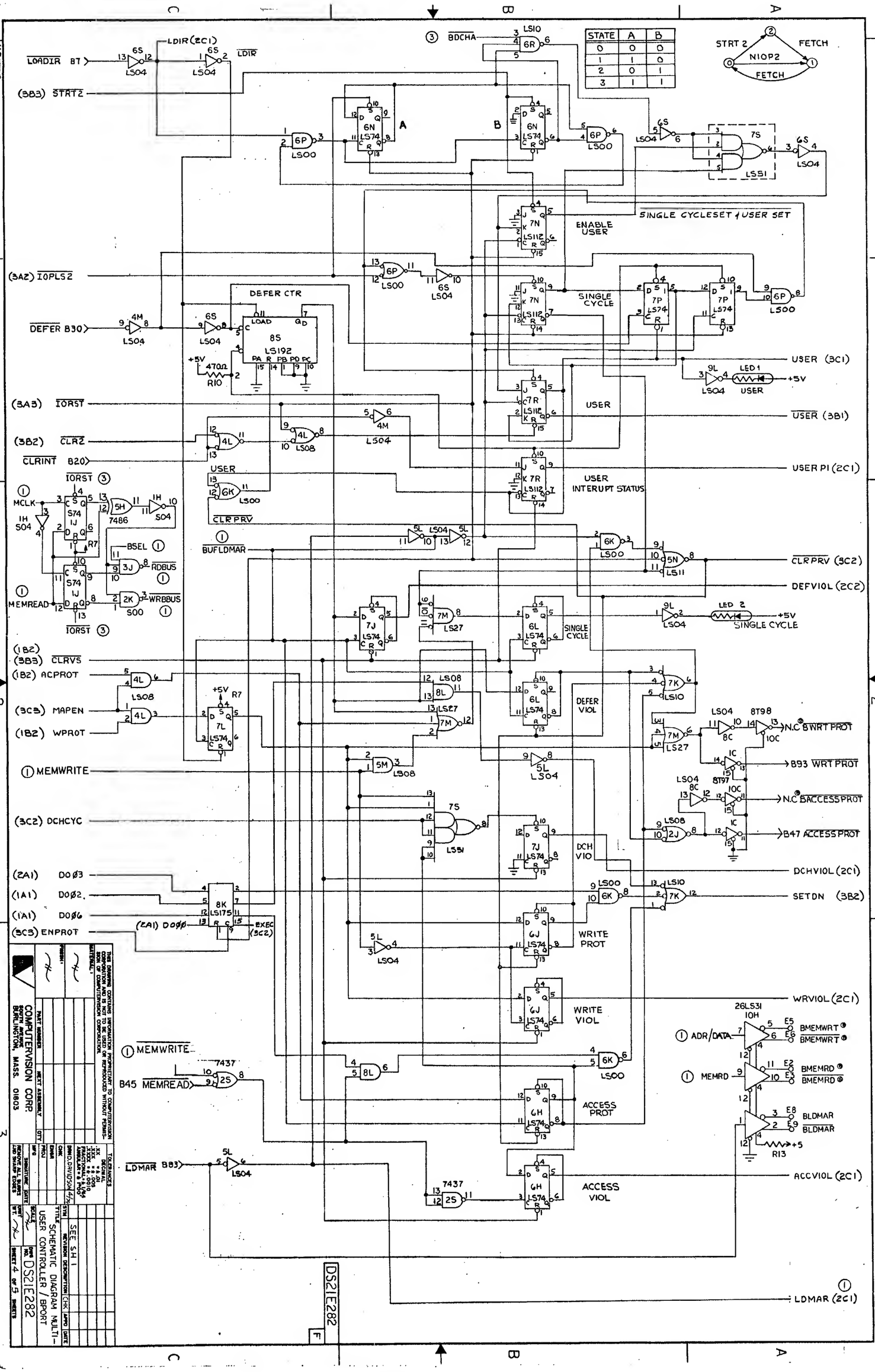
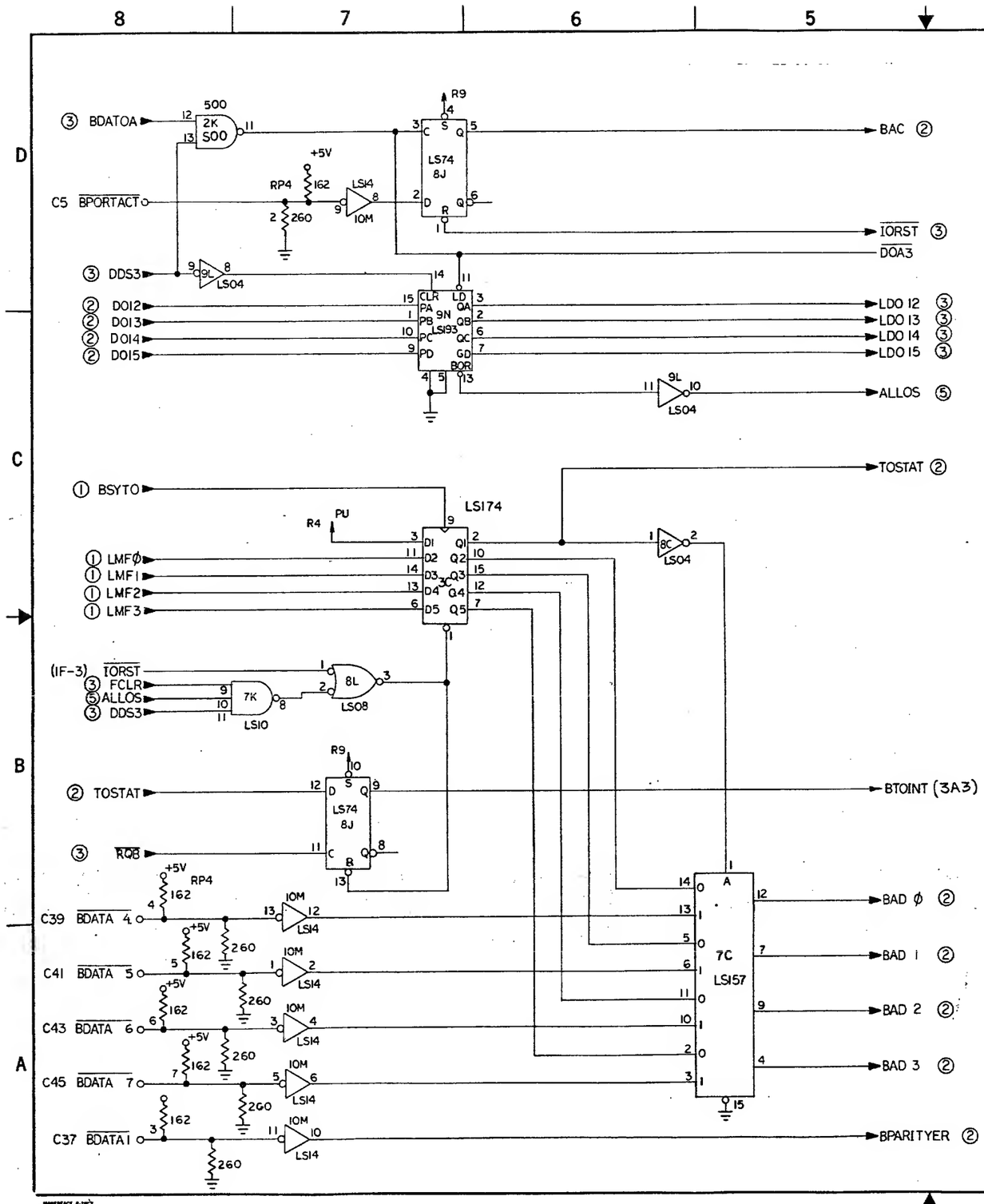
TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'
DRWN D. DAVIDSON 4/79
SEE SH 1
REVISION DESCRIPTION CHK APPD DATE
TITLE SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT
PART NUMBER NEXT ASSEMBLY QTY
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
SCALE
DWG NO. DS21E282
SHEET 3 OF 5 SHEETS



STATE A B
0 0 0
1 1 0
2 0 1
3 1 1
STRT 2
FETCH
N10P2
FETCH
LOADIR B7
LDIR (2C1)
LDIR
(3B3) STRT2
BDCHA
(3A2) IOPLS2
DEFER B30
DEFER CTR
8S
LS192
(3A3) IORST
(3B2) CLR2
CLRINT B20
IORST
MCLK
MEMREAD
BSEL
RDBUS
WRBBUS
(1B2)
(3B3) CLRVS
(1B2) ACPROT
(3C3) MAPEN
(1B2) WPROT
MEMWRITE
(3C2) DCHCYC
(2A1) D0Ø3
(1A1) D0Ø2
(1A1) D0Ø6
(3C3) ENPROT
(2A1) D0ØØ
EXEC (3C2)
MEMWRITE
B45 MEMREAD
LDMAR B83
ENABLE USER
SINGLE CYCLESET / USER SET
SINGLE CYCLE
USER
USER INTERUPT STATUS
USER (3C1)
USER (3B1)
USER P1 (2C1)
CLRPRV (3C2)
DEFVIOL (2C2)
SINGLE CYCLE
DEFER VIOL
DCH VIO
WRITE PROT
WRITE VIOL
ACCESS PROT
ACCESS VIOL
N.C. BWRT PROT
B93 WRT PROT
N.C. BACCESS PROT
B47 ACCESS PROT
DCHVIOL (2C1)
SETDN (3B2)
WRVIOL (2C1)
ADR/DATA
MEMRD
BMEMWRT
BMEMRD
BLDMAR
ACCVIOL (2C1)
LDMAR (2C1)
DS21E282
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT
SEE SH 1
DS21E282
SHEET 4 OF 5 SHEETS



SWITCH PACKS 5D & 5F

THE PRORER SWITCHES IN SWITCH PACKS 5D & 5F MUST BE CLOSED WHEN THE MUC IS DRIVING BPORT MEMORIES. ONE SWITCH MUST BE CLOSED FOR EVERY 32K BPORT FIELD SEGMENT ADDRESS THAT IS BEING USED IN A CONFIGURED SYSTEM.

BPORT FIELD ADDR*	CLOSED SWITCH POSITION 5D	5F
0		8
1		7
2		6
3		5
4		4
5		3
6		2
7		1
8	8	
9	7	
10	6	
11	5	
12	4	
13	3	
14	2	
15	1	

* THE BPORT FIELD ADDR REPRESENTS ONE 32K SEGMENT OF MEMORY.

REF SHT.2, JP1 MUST BE INSERTED WHEN THE MUC IS DRIVING BPORT MEMORIES.

BPORT CONNECTOR PINOUTS

CONN C

1	BINTR		2
3			4
5	BPORTACT		6
7			8
9			10
11	BIORST		12
13	BCLR		14
15	BIOPLS		16
17			18
19	BDS3		20
21	BDS2		22
23	BDS1		24
25	BDS0		26
27			28
29			30
31	BRQENB		32
33			34
35			36
37	BDATA1		38
39	BDATA4		40
41	BDATA5		42
43	BDATA6		44
45	BDATA7		46
47			48
49			50

CONN E

1		BMEMRD	2
3	BMEMRD		4
5	BMEMWRT	BMEMWRT	6
7		BLDMAR	8
9	BLDMAR		10
11	BMEMBUS15		12
13	14		14
15	13		16
17	12		18
19	11		20
21	10		22
23	9		24
25	8		26
27	7		28
29	6		30
31	5		32
33	4		34
35	3		36
37	2	FREE	38
39	1	FREE	40
41	BMEMBUSØ		42
43	BMC3	FREE	44
45	BMC2	BMC Ø	46
47	BMC1		48
49		BMEMBSY	50

ALL UNUSED PINS GROUNDED

DS21E282 E

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MATERIAL:

FINISH:

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

DRN P. Magee 2/79
CHK
ENGR
PROJ
MFG
SIGNATURE | DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SH 1

SYM | REVISION DESCRIPTION | CHK | APPD | DATE

TITLE SCHEMATIC DIAGRAM MULTI-USER CONTROLLER / BPORT

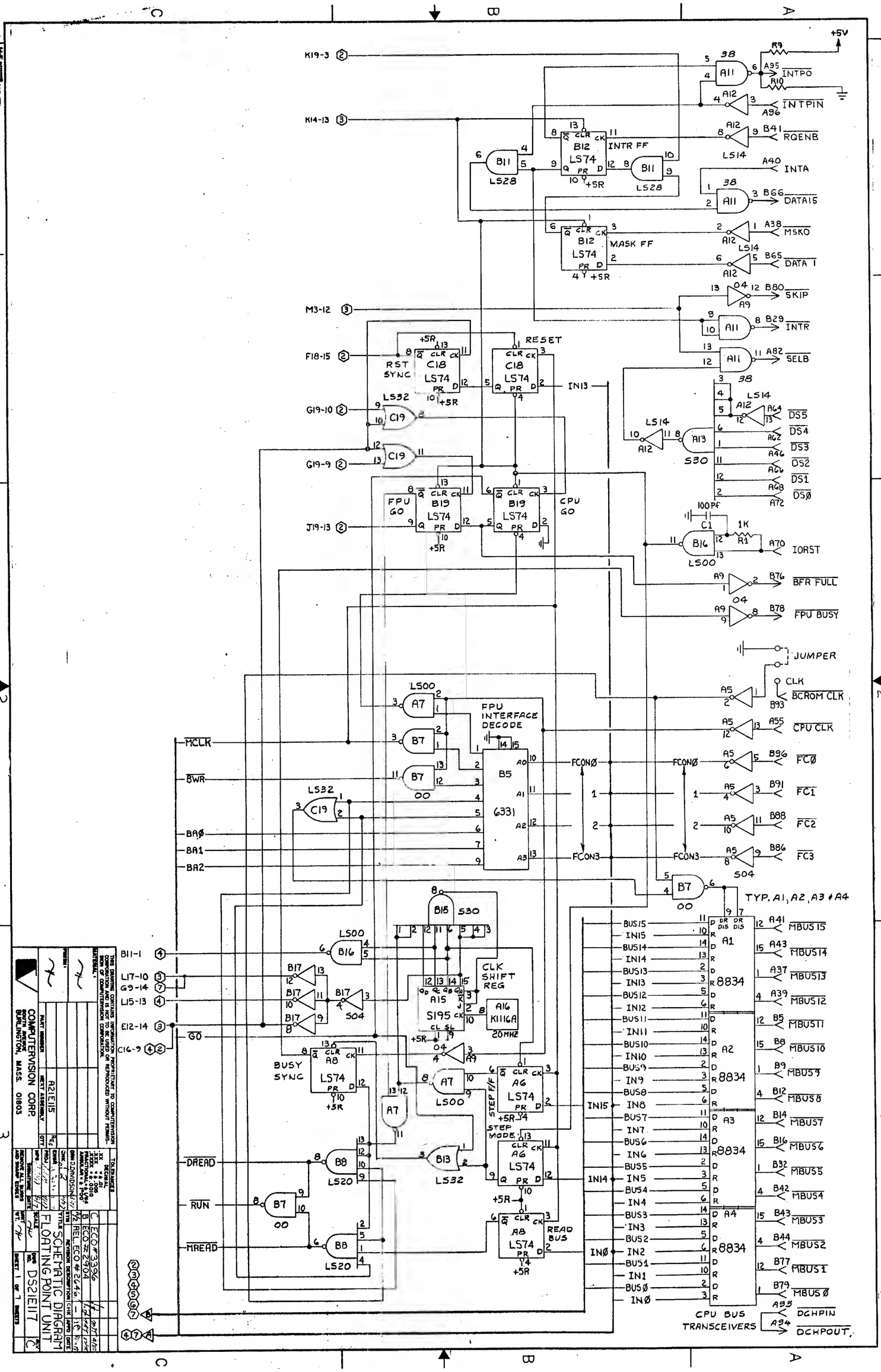
SCALE — DWG NO. DS21E282

UNIT WT. —

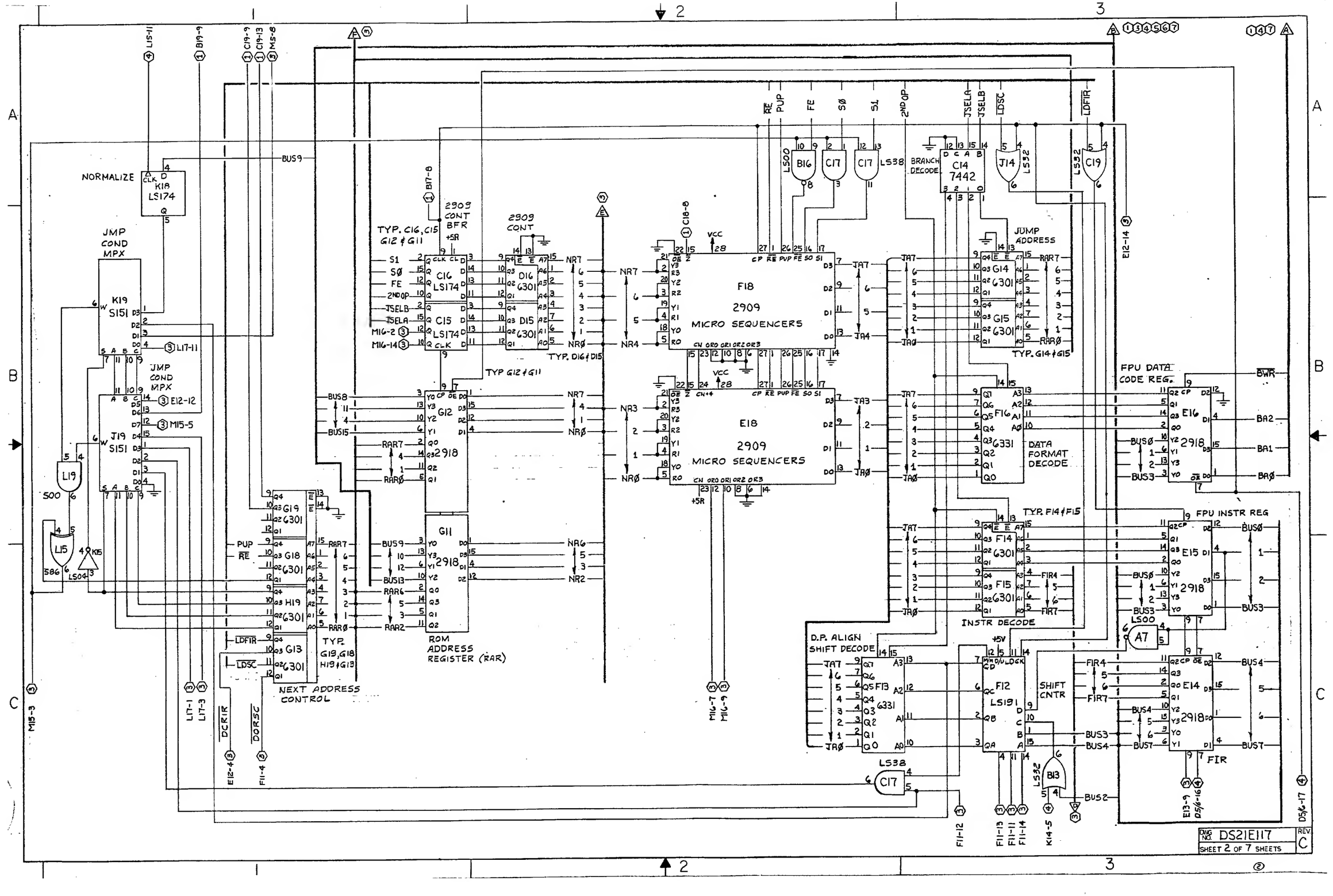
SHEET 5 OF 5 SHEETS

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

Floating Point Unit



+5V
K19-3
K14-13
M3-12
F18-15
G19-10
G19-9
J19-13
INTPO
INTPIN
RQENB
INTA
DATA15
MSKO
DATA 1
SKIP
INTR
SELB
INTR FF
MASK FF
RESET
RST SYNC
FPU GO
CPU GO
DS5
DS4
DS3
DS2
DS1
DSØ
IORST
BFR FULL
FPU BUSY
JUMPER
CLK
BCROM CLK
CPU CLK
FCØ
FC1
FC2
FC3
FPU INTERFACE DECODE
6331
MCLK
BWR
BAØ
BA1
BA2
FCONØ
FCON3
TYP. A1, A2, A3 & A4
MBUS15
MBUS14
MBUS13
MBUS12
MBUS11
MBUS10
MBUS9
MBUS8
MBUS7
MBUS6
MBUS5
MBUS4
MBUS3
MBUS2
MBUS1
MBUSØ
DCHPIN
DCHPOUT
CPU BUS TRANSCEIVERS
CLK SHIFT REG
20MHZ
BUSY SYNC
STEP F/F
STEP MODE
READ BUS
B11-1
L17-10
G9-14
L15-13
E12-14
C16-9
GO
DREAD
RUN
MREAD
COMPUTERVISION CORP.
SOUTH AVENUE
BURLINGTON, MASS. 01803
A21E115
SCHEMATIC DIAGRAM
FLOATING POINT UNIT
DS21E117
C ECO #3396
B ECO #2904
A REL. ECO #2646


NORMALIZE
K18 LS174
JMP COND MPX
K19 S151
J19 S151
L19
L15
K15
LS04
2909 CONT BFR
TYP. C16, C15 G12 & G11
2909 CONT
C16 LS174
C15 LS174
D16 6301
D15 6301
TYP. D16 & D15
TYP G12 & G11
G12 2918
G11 2918
ROM ADDRESS REGISTER (RAR)
G19 6301
G18 6301
H19 6301
G13 6301
TYP. G19, G18 H19 & G13
NEXT ADDRESS CONTROL
F18 2909 MICRO SEQUENCERS
E18 2909 MICRO SEQUENCERS
BRANCH DECODE
C14 7442
J14
C19
JUMP ADDRESS
G14 6301
G15 6301
TYP. G14 & G15
F16 6331
DATA FORMAT DECODE
FPU DATA CODE REG.
E16 2918
FPU INSTR REG
E15 2918
TYP. F14 & F15
F14 6301
F15 6301
INSTR DECODE
D.P. ALIGN SHIFT DECODE
F13 6331
F12 LS191
SHIFT CNTR
E14 2918
FIR
A7
B13
C17
DCRIR
DORSC
DWG NO. DS21E117
SHEET 2 OF 7 SHEETS
REV. C

CLOCK AND STATUS CONTROL

TYP. G16, G17, H14, H15, H16, H17 & H18

RALU CLOCK CONTROL

TYP. D17, D18 & D14

2901 SOURCE CONTROL

B SELECT MULTIPLEX

A SELECT MULTIPLEX

TYP. D13, D11 & D12 2901 ADDRESS CONTROL

TYP. C12 & C13

SHIFT COUNTER

FIR & REG COUNTER

FIR GATE

BUS CONTROL

NEXT ADDRESS OR

A SIGN

B SIGN

SKIP REG.

SKIP DECODE

OVER-FLOW SAVE

UNDERFLOW SAVE

STATUS LD MPX

STATUS BUS GATE

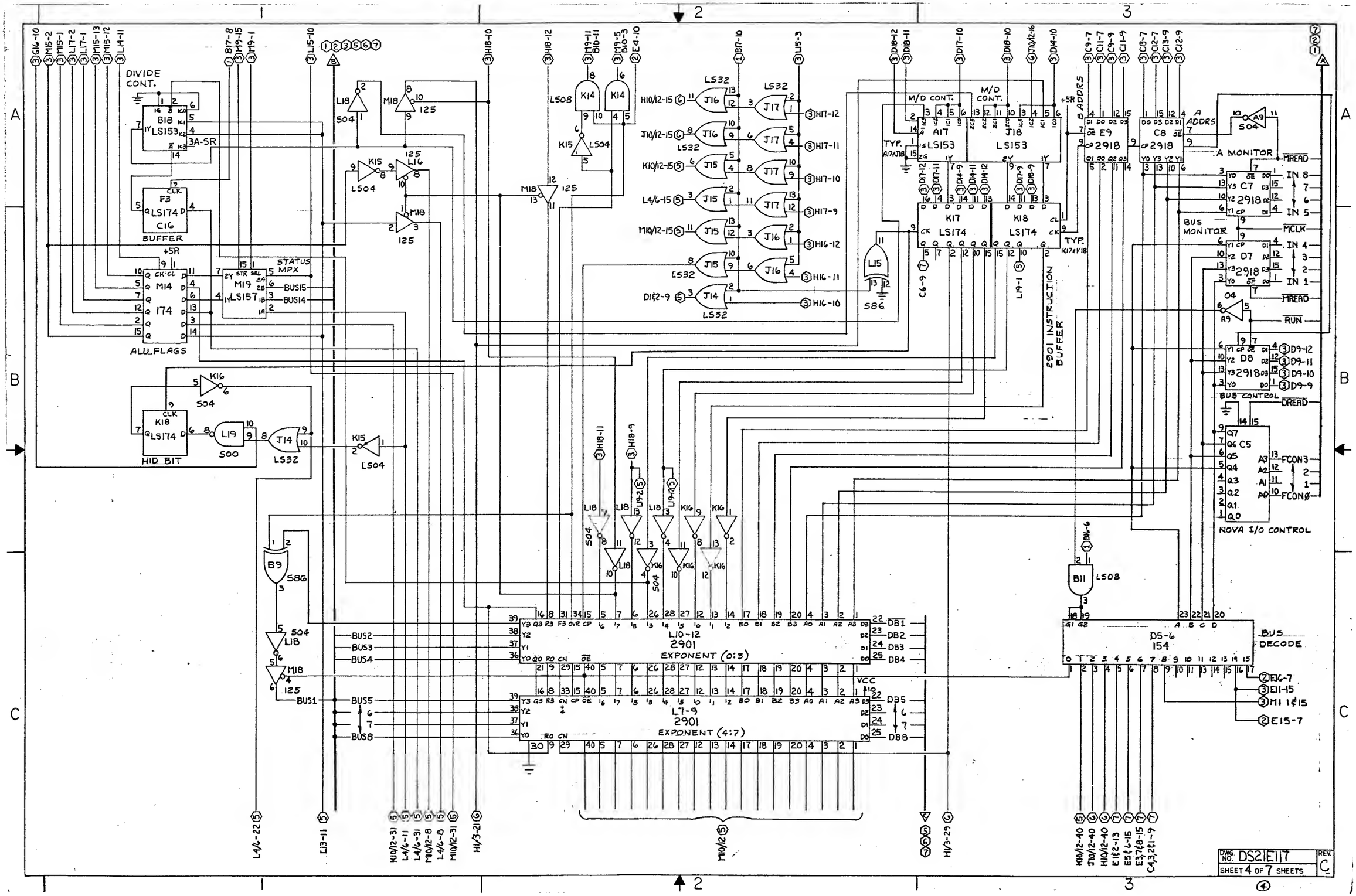
UNDERFLOW

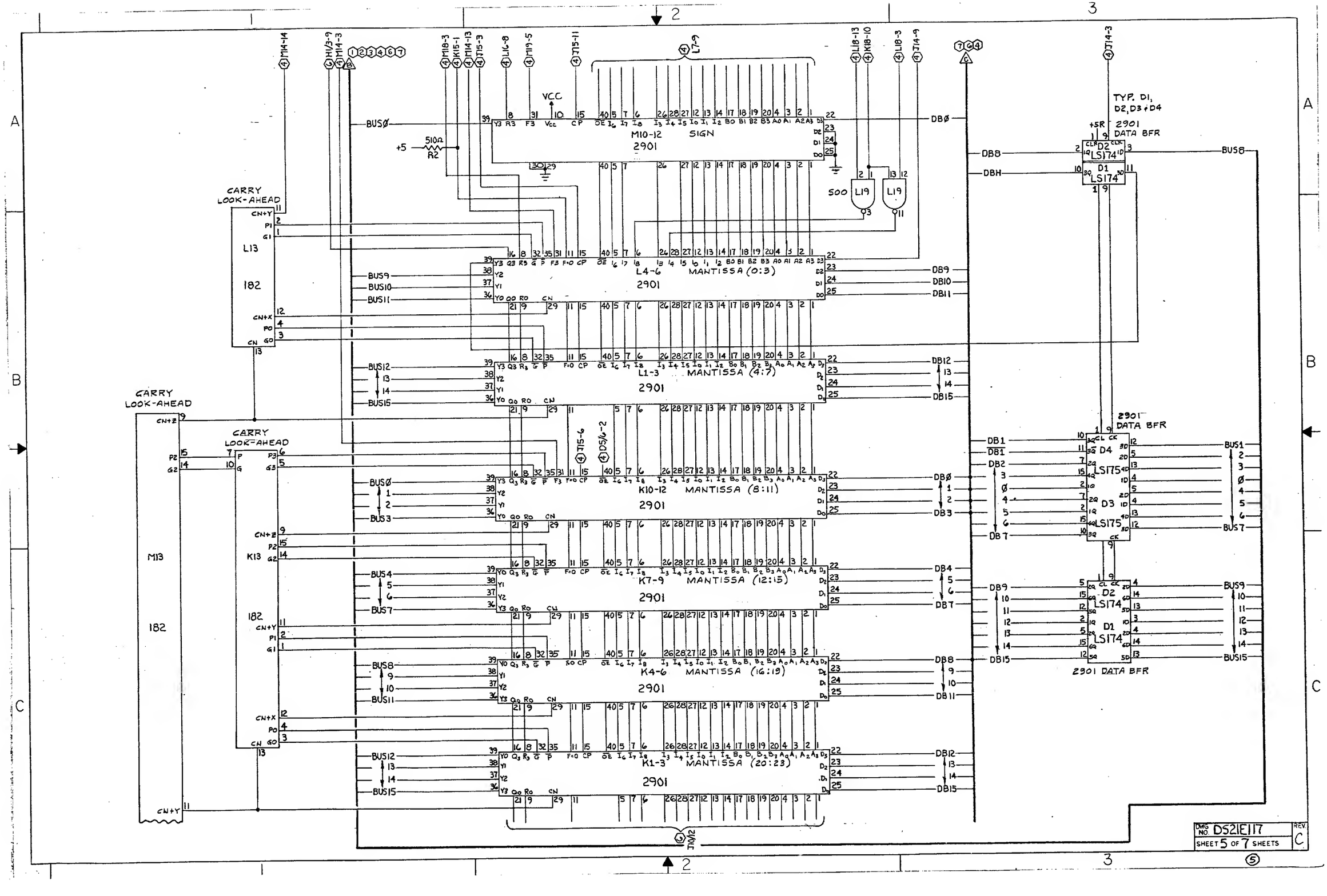
OVERFLOW

TYP. C9 & C11

TYP. M1, M4, M8

DWG. NO.	D521E117
REV.	C
SHEET	3 OF 7 SHEETS


DIVIDE CONT.
BUFFER
ALU FLAGS
STATUS MPX
HID BIT
M/D CONT.
2901 INSTRUCTION BUFFER
A MONITOR
BUS MONITOR
BUS CONTROL
NOVA I/O CONTROL
BUS DECODE
EXPONENT (0:3)
EXPONENT (4:7)
DWG. NO. DS21E117
SHEET 4 OF 7 SHEETS
REV. C



M10-12 SIGN
2901
L4-6 MANTISSA (0:3)
2901
L1-3 MANTISSA (4:7)
2901
K10-12 MANTISSA (8:11)
2901
K7-9 MANTISSA (12:15)
2901
K4-6 MANTISSA (16:19)
2901
K1-3 MANTISSA (20:23)
2901
CARRY LOOK-AHEAD
L13
182
M13
182
K13
182
TYP. D1, D2, D3 & D4
2901 DATA BFR
D2 LS174
D1 LS174
D4 LS175
D3 LS175
2901 DATA BFR
2901 DATA BFR
VCC
+5
510Ω R2
500
L19
L19
BUSØ
BUS9
BUS10
BUS11
BUS12
BUS15
BUSØ
BUS3
BUS4
BUS7
BUS8
BUS11
BUS12
BUS15
DBØ
DB8
DBH
DB9
DB10
DB11
DB12
DB15
DB1
DB2
DB7
DB9
DB15
BUS8
BUS1
BUS7
BUS9
BUS15
DWG NO. DS21E117
SHEET 5 OF 7 SHEETS
REV. C

CARRY LOOK-AHEAD

M13

182

J13

182

CARRY LOOK-AHEAD

H13

182

J10-12 2901 MANTISSA (24:27)

J7-9 2901 MANTISSA (28:31)

J4-6 2901 MANTISSA (32:35)

J1-3 2901 MANTISSA (36:39)

H10-12 2901 MANTISSA (40:43)

H7-9 2901 MANTISSA (44:47)

H4-6 2901 MANTISSA (48:51)

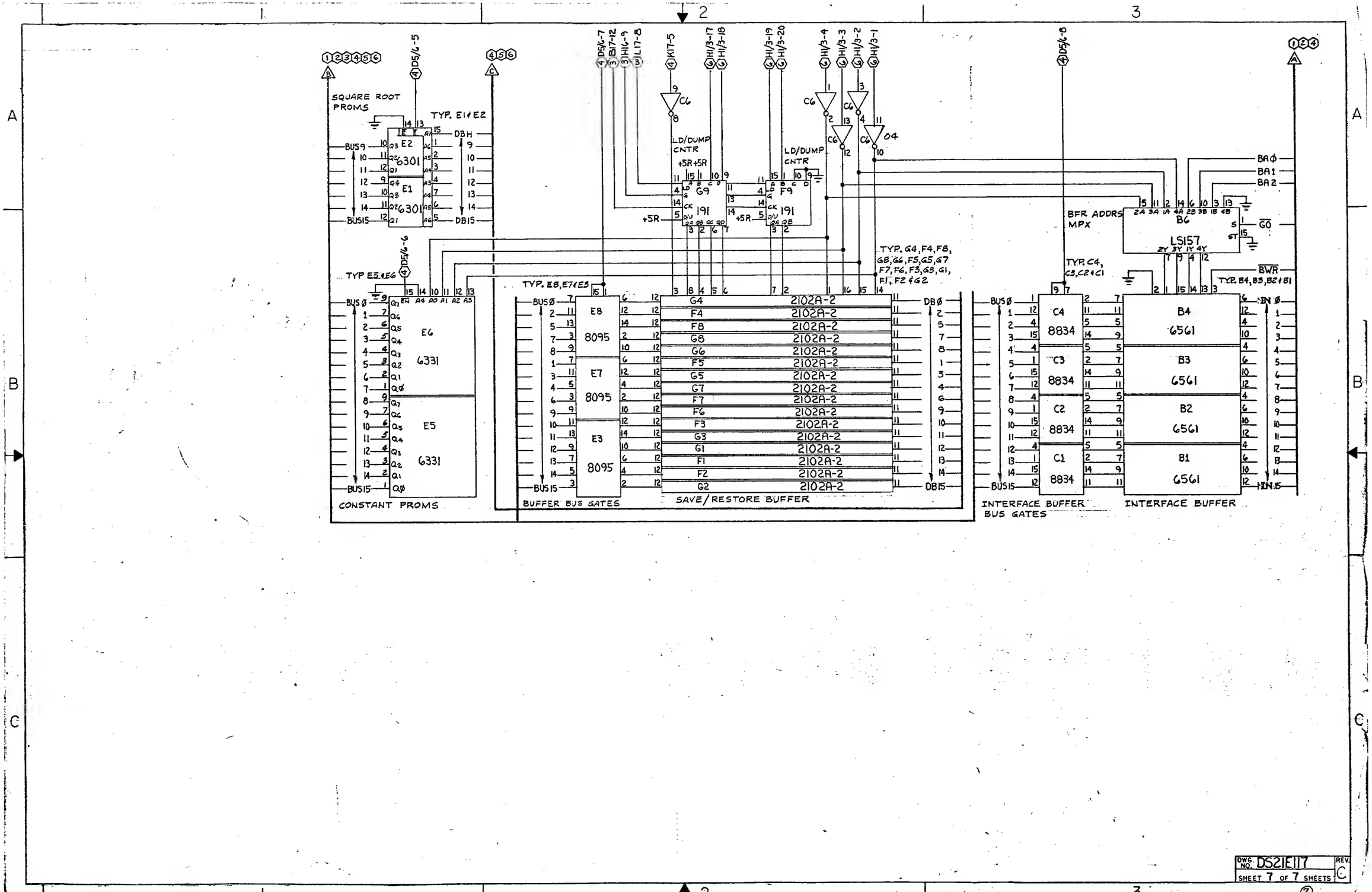
H1-3 2901 MANTISSA (52:55)

BUSØ BUS3 BUS4 BUS7 BUS8 BUS11 BUS12 BUS15

DBØ DB3 DB4 DB7 DB8 DB11 DB12 DB15

VCC

G9-10 G9-9 F9-15 F9-1 C9-1 C6-13 C6-3 C6-11


SQUARE ROOT PROMS
TYP. E1 & E2
E2 6301
E1 6301
BUS9
BUS15
DBH
DB15
D5/6-5
D5/6-6
TYP E5 & E6
E6 6331
E5 6331
CONSTANT PROMS
D5/6-7
B17-12
H16-9
L17-8
K17-5
H1/3-17
H1/3-18
H1/3-19
H1/3-20
H1/3-4
H1/3-3
H1/3-2
H1/3-1
C6
LD/DUMP CNTR
+5R
G9 191
F9 191
TYP. E8, E7 & E3
E8 8095
E7 8095
E3 8095
BUFFER BUS GATES
TYP. G4, F4, F8, G8, G6, F5, G5, G7, F7, F6, F3, G3, G1, F1, F2 & G2
G4 2102A-2
F4 2102A-2
F8 2102A-2
G8 2102A-2
G6 2102A-2
F5 2102A-2
G5 2102A-2
G7 2102A-2
F7 2102A-2
F6 2102A-2
F3 2102A-2
G3 2102A-2
G1 2102A-2
F1 2102A-2
F2 2102A-2
G2 2102A-2
DBØ
DB15
SAVE/RESTORE BUFFER
D5/6-8
BFR ADDRS MPX
B6 LS157
BAØ
BA1
BA2
GO
BWR
TYP. C4, C3, C2 & C1
TYP. B4, B3, B2 & B1
C4 8834
C3 8834
C2 8834
C1 8834
INTERFACE BUFFER BUS GATES
B4 6561
B3 6561
B2 6561
B1 6561
INTERFACE BUFFER
DWG. NO. DS21E117
REV. C
SHEET 7 OF 7 SHEETS

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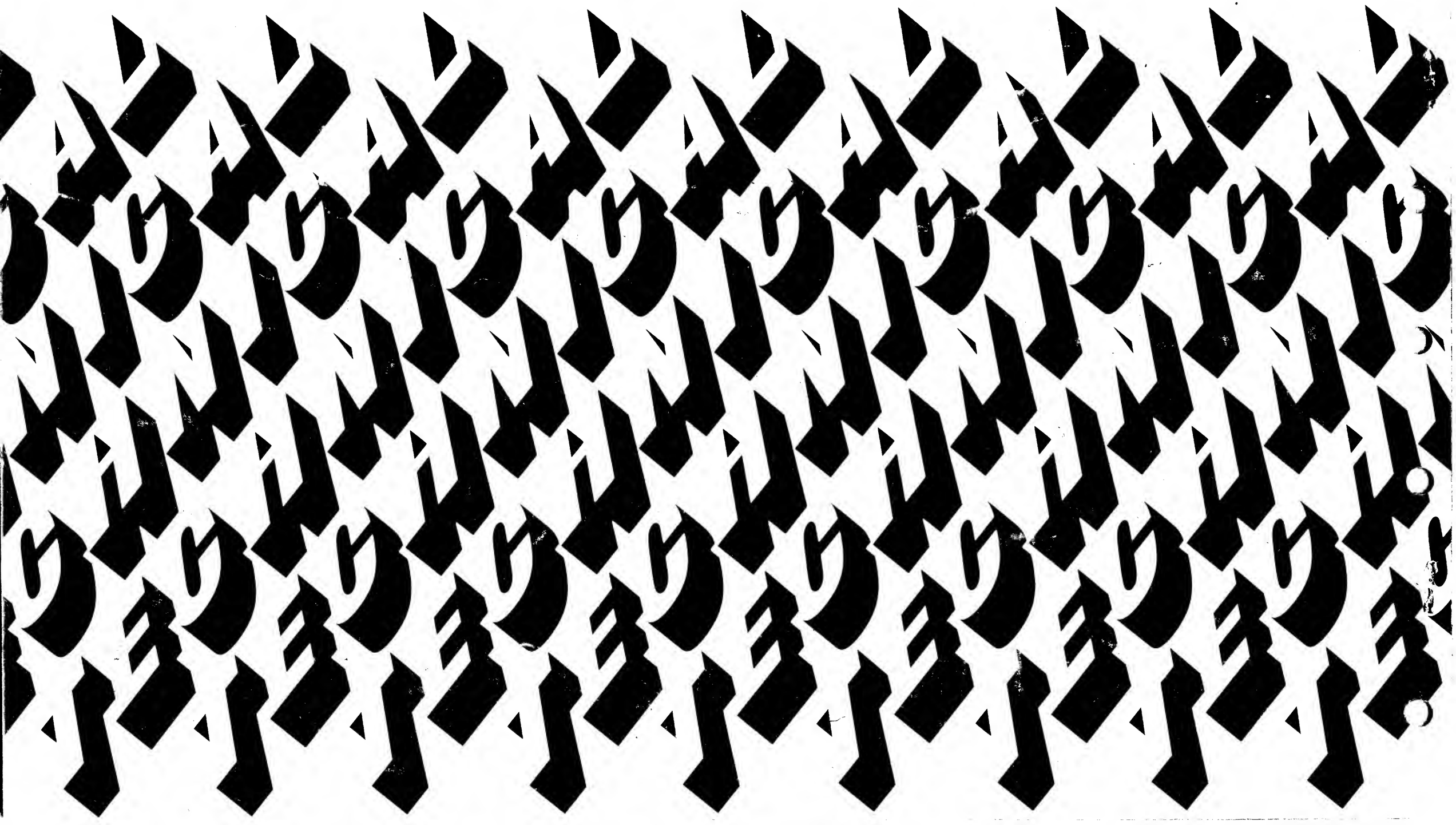
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